

# sample approved sheet

Model No : ☐ MD101-009TDANWW ☐ MD101-009TDANGW

☐ MD101-009TDAN (上光下光)

Customer: \_\_\_\_\_

Version:                     D                    

Date:                     2010-11-26                    

**CUSTOMER'S Accept APPROVAL&DATE:** \_\_\_\_\_

## CUSTOMER'S APPROVAL :

**A.Configuration:** ☐ OK ☐ NG

**B.Function:** ☐ OK ☐ NG

**C.Standard for product check:** ☐ OK ☐ NG

**D.Other:** ☐ OK ☐ NG

**CUSTOMER'S SIGNATURE &DATE:** \_\_\_\_\_

For improve, please tick or explain it(them) as belows while on debugging on our products:

☐ A. price away from our target: \_\_\_\_\_

☐ B. other supply's debugging success: \_\_\_\_\_

☐ C. Sample period away from our target: \_\_\_\_\_

☐ D. Project cancel : \_\_\_\_\_

☐ E. NO need to test for solution change: \_\_\_\_\_

☐ F. Other: \_\_\_\_\_

**Engineering by :**

**Quality by :**

**Approvedby :**

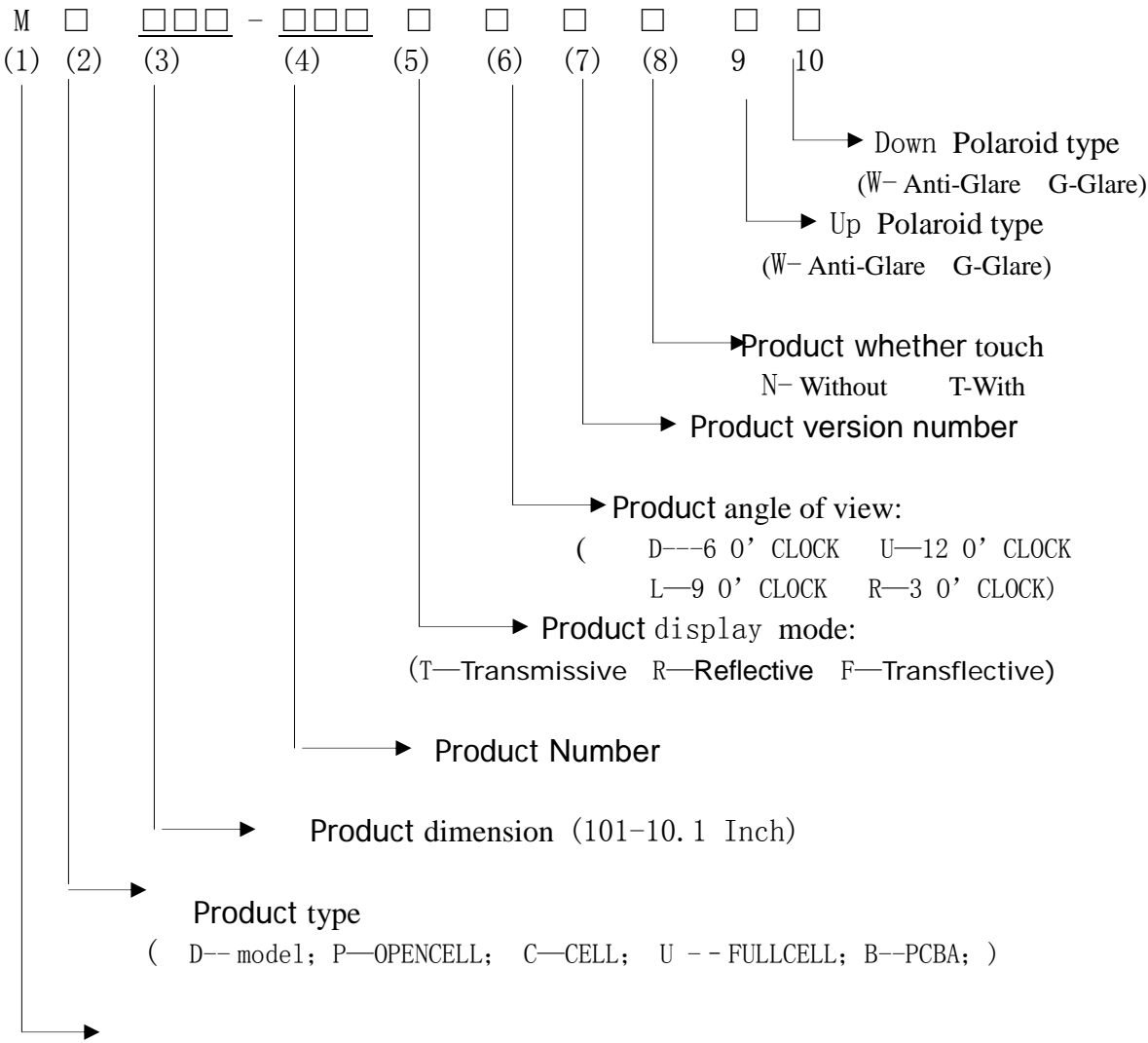
# Product Specification

<b>Product</b>	<p>Standard LCD Module</p> <p>1024(RGB) x 600Dots graphic type</p> <p>10.1" TFT 262K Transmissive LCD</p> <p>COG bonding type</p> <p>Wide temperature</p> <p>LED back light</p> <p>Without Touch Panel</p> <p>LVDS interface</p>
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变更记录

日期	版本	修改 页码	变更前描述	变更后描述	备注
2010-11-24	C	13	VLED Min: 2.5	VLED Min: 4.5	
2010-11-24	C	13	FPWM	Typ.200Hz	

Product **Model description**



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# 1. Summary

This technical specification applies to 10.1" color TFT-LCD is a color active matrix thin film transistor (TFT) liquid crystal display(LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has a 10.1-inch diagonally measured active display area with WSVGA resolution (1024 vertical by 600 horizontal pixel array)

## 2. Features

- 10.1" WSVGA TFT LCD Panel
- LED Light-bar Backlight System
- Supported WSVGA (V:1024 lines, H:600 pixels) Resolution
- DualGate(2 Source + 2Gate)

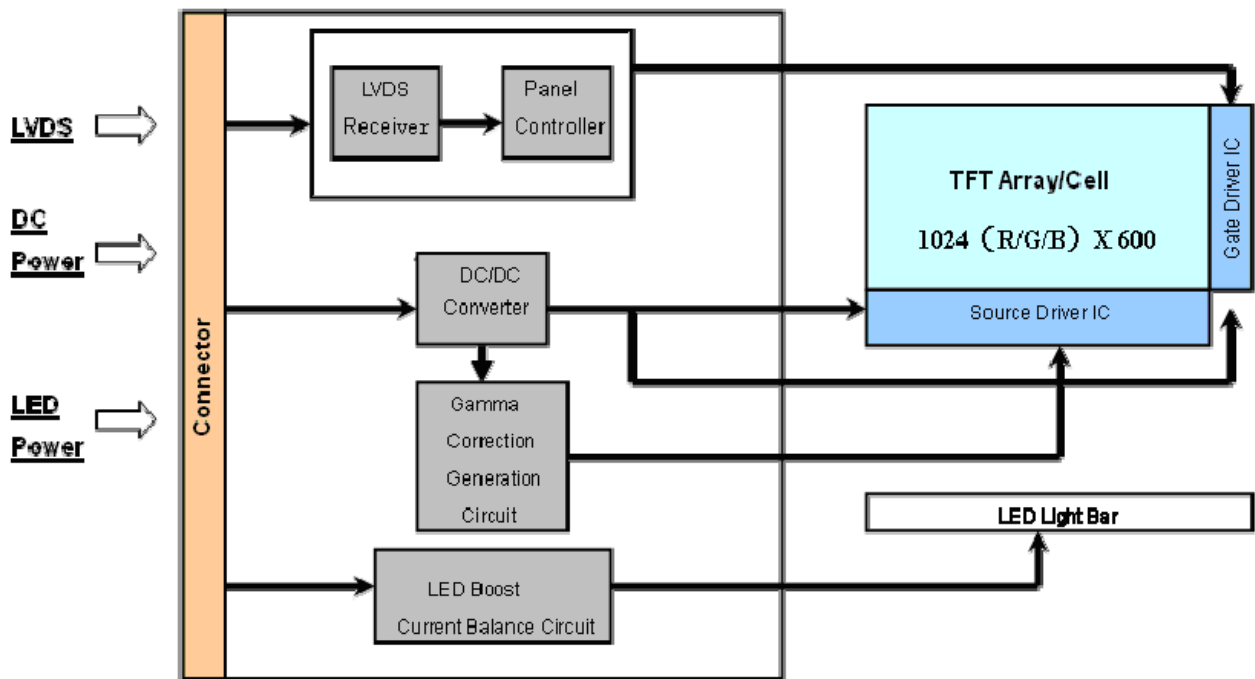
## 3.General Specifications

NO	Item	Contents	Contents	Unit
(1)	Module Outsize(mm)	235 x 143 x 5.2(Typ.)		mm
(2)	LCD Active area(mm)	222.72(H) x 125.28(V)		mm
(3)	Display resolution(dot)	1024(x3) x 600		dot
(4)	Screen size(inch)	10.1		Inch
(5)	Dot pitch(mm)	0.2175(H) x 0.2088(V)		mm
(6)	Color configuration	R.G. B vertical stripe		-
(7)	Support color	262 K		-
(8)	Display Mode	Normally White(TN)		-
(9)	Gray Scale inversion	6 O'Clock		-
(10)	LCD type	a-si TFT		-
(11)	Electrical Interface(Logic)	LVDS		-
(12)	Weight	TBD		g
(13)	Panel surface treatment	Anti-Glare	MD101-009TDANWW	-
		Glare	MD101-009TDANGW	
(14)	White Luminance	200 (Typ.)	5 points average	Cd/m2
(15)	Contrast Ratio	500 (Typ.)		
(16)	VDD Input Voltage(V)	+3.3 (Typ.)	3.0 (Min.) ~3.6 (Max.)	V
(17)	Power Consumption(W)	0.96(Typ.)		watt

# 4.Function Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

Figure 1 Block diagram



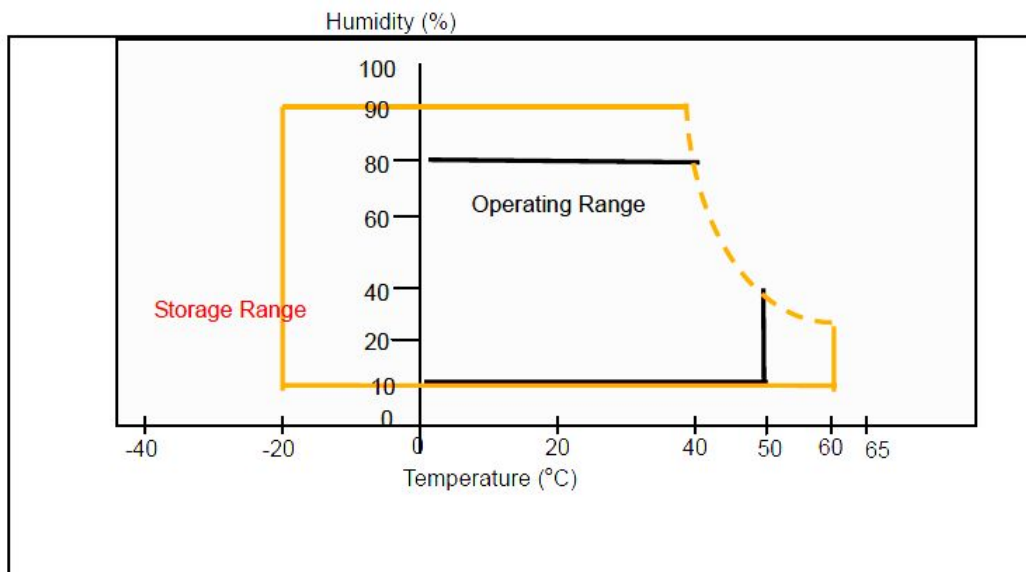
## 5.Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Condition
Supply Voltage	VDD	-0.3	3.6	V	Typ.=3.3V
Supply V_LED voltage	V_LED	4.5	5.5	V	Typ.=5V
Input Signal		-0.3	2.7	v	LVDS signals
Operating Temperature	TOP	0	50	deg. C	(Note 3 )
Operating Humidity	HOP	10	80	%RH	(Note 3 )
Storage Temperature	TST	-20	60	deg. C	(Note 3 )
Storage Humidity	HST	10	90	%RH	(Note 3 )
Vibration	-	-	1.5G 10~500Hz	G Hz	30min for X, Y, Z axis
Shock	-	-	220 2	G ms	Half sign wave
LED Current	I_LED	-	20	mA	per LED

### Note:

- (1) Maximum Wet-Bulb should be 39 degree C. No condensation.
- (2) When you apply the LCD module for OA system. Please make sure to keep the temperature of LCD module is less than 60°C.
- (3) Storage /Operating temperature.

### Relative Humidity(%RH)

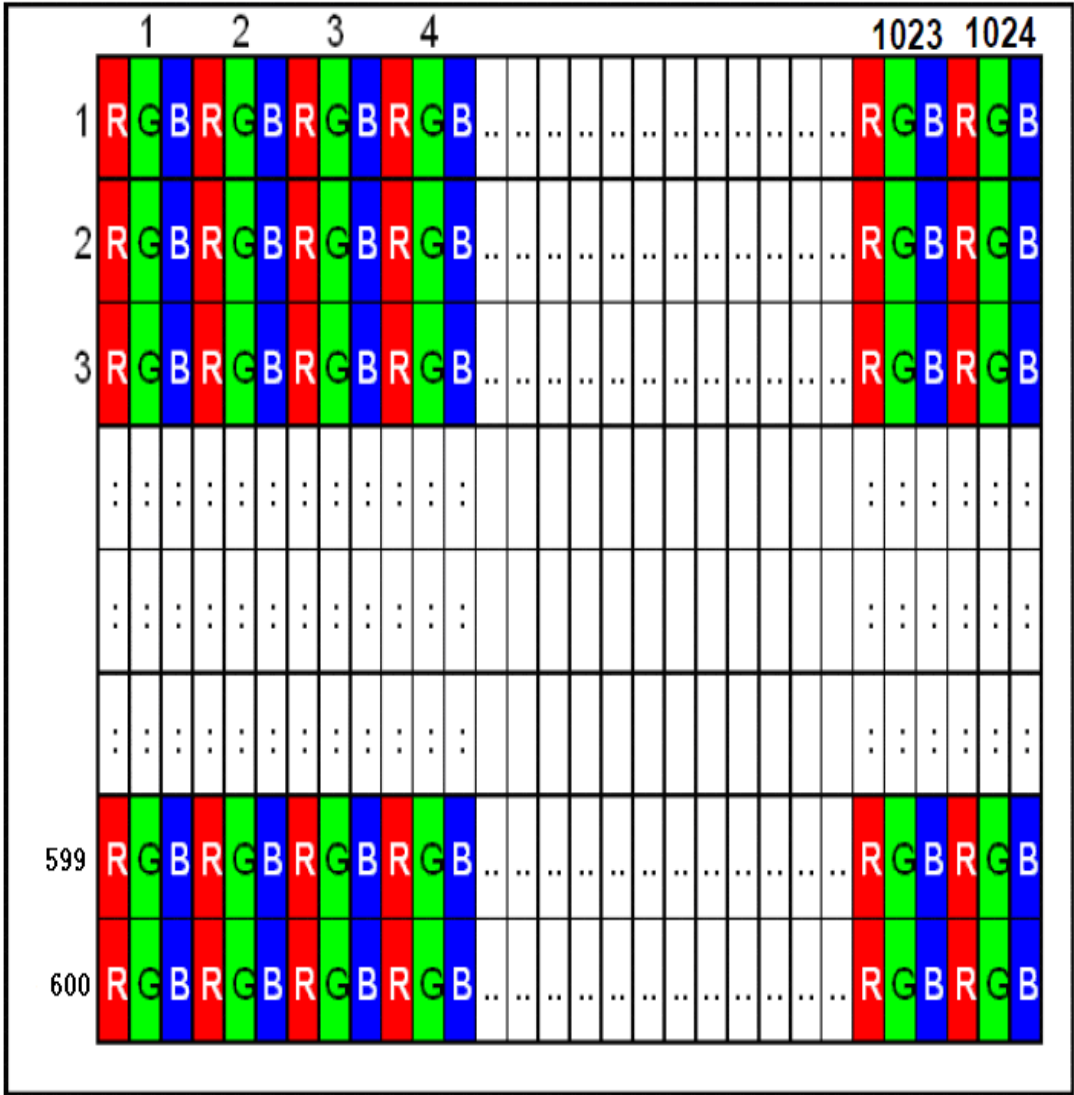




# 6.Pixel Format Image

Figure 2 shows the relationship of the input signals and LCD pixel format image.

Figure 2 Pixel Format



## 7.Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

**Table 2 Optical Characteristics**

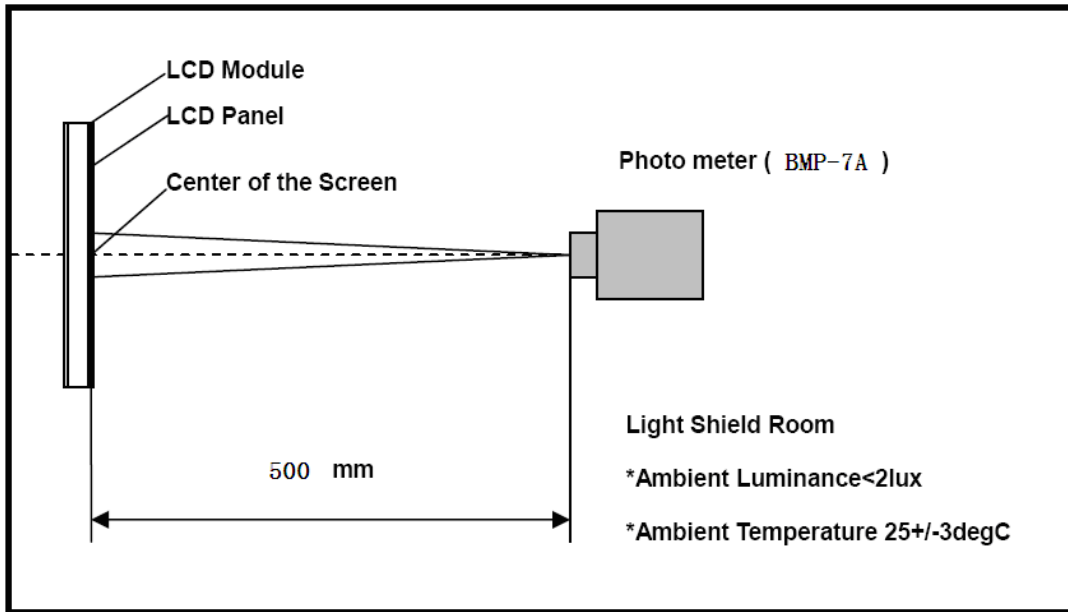
Item	Conditions		Specification			
			Min.	Typ.	Max.	Note
Viewing Angle [degrees] K=Contrast Ratio>10	Horizontal	Left	40	45	-	A,B
		Right	40	45	-	
	Vertical	Up	10	15	-	
		Down	30	35	-	
Contrast ratio	Center		450	--	--	A,C
Response Time [ms]	Rising + Falling		-	3+5	16	A,D
Color Chromaticity (CIE1931)	Red x		Typ. -0.03	0.564	Typ. +0.03	A,
	Red y			0.327		A,
	Green x			0.336		A,
	Green y			0.578		A,
	Blue x			0.151		A,
	Blue y			0.103		A,
	White x			0.290		A,
	White y			0.316		A,
White Luminance [cd/m^2]	I-LED=20.0mA		150	180		5point A, E
Luminance Uniformity [%]	I-LED=20.0mA 13points		-	-	-	A, F
	I-LED=20.0mA 5points		80	-	-	

### Note:

#### A. Measurement Setup

The LCD module should be stabilized at given temperature for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

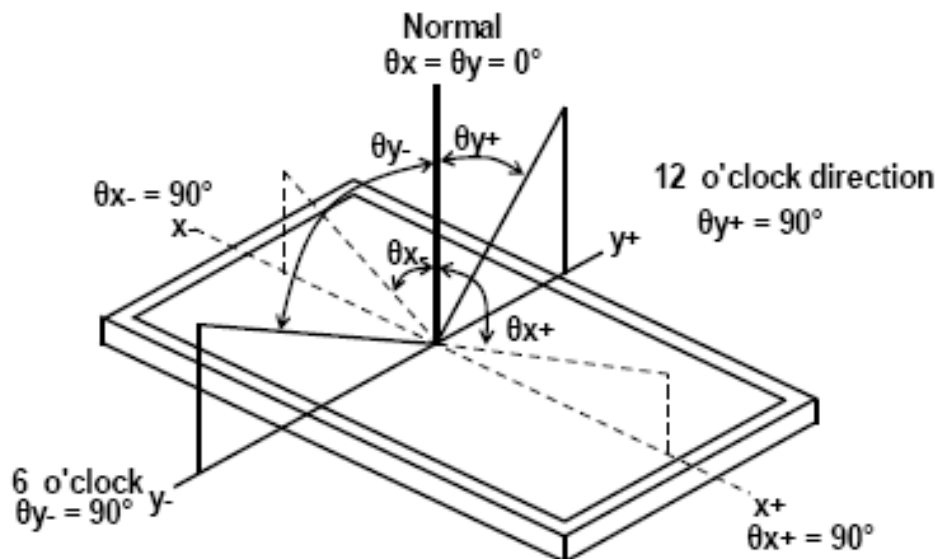
**Figure 3 Measurement Setup**



**B. Definition of**

### Viewing Angle

**Figure 4 Definition of Viewing Angle**



### C. Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

L63: Luminance of gray level 63, L0: Luminance of gray level 0

#### D. Definition of Response Time (TR, TF)

Figure 5 Definition of Response Time

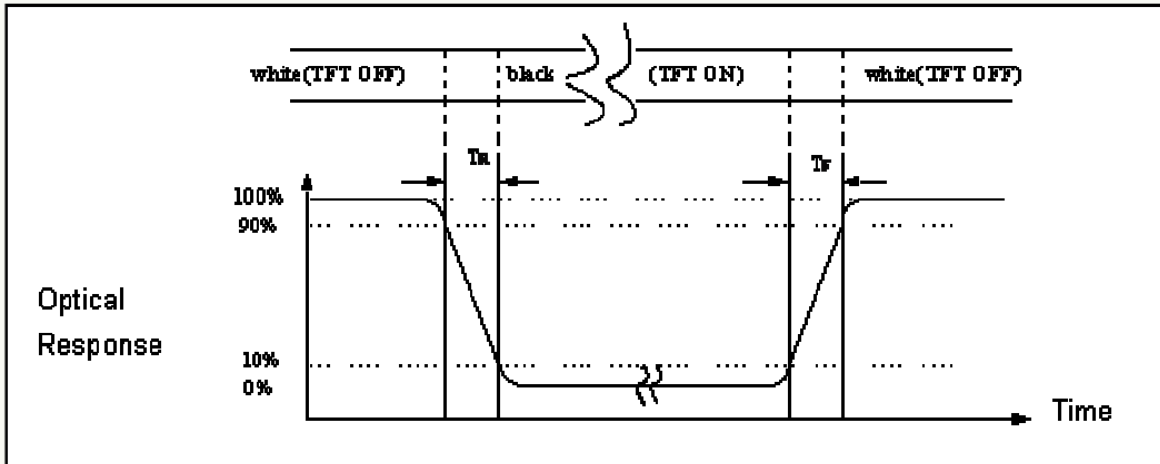
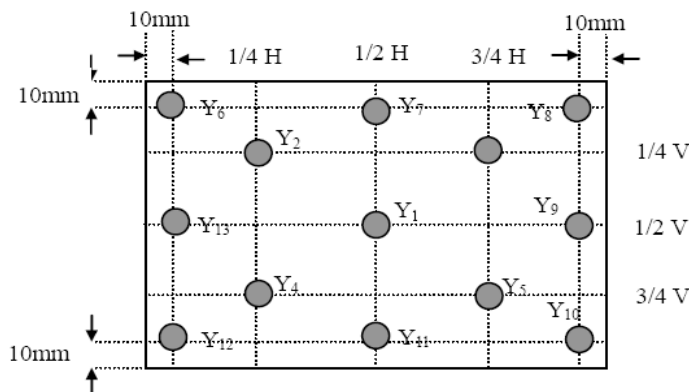


Figure 6 Measurement Locations of 13 Points



#### E. Definition of Luminance White

Measure the luminance of gray level 63 at center point and 5 points.

Center of Luminance = Y1

Average Luminance of 5 points =  $(Y1 + Y2 + Y3 + Y4 + Y5)/5$

#### F. Definition of Luminance Uniformity(Variation)

Measure the luminance of gray level 63 at 13 points.

$$\text{Uniformity of 13 points} = \frac{\text{Min Luminance of Y1~Y13}}{\text{Max Luminance of Y1~Y13}} \times 100\%$$

$$\text{Uniformity of 5 points} = \frac{\text{Min Luminance of Y1~Y5}}{\text{Max Luminance of Y1~Y5}} \times 100\%$$

## 8.Backlight Characteristics

### 8.1 Parameter Guideline of LED Backlight

**Table 3 Parameter Guideline for LED Backlight**

Symbol	Parameter		Min.	Typ.	Max.	Units	Condition
VLED	LED input		4.5	5	5.5	V	Ta=25℃
VF	LED Light bar Driving		9.0	9.6	10.5	V	Ta=25℃
IF	LED Current		-	180	-	mA	Ta=25℃
PLED	LED Power Consumption					W	Ta=25℃
LT	LED Life Time		10000	-	-	Hours	T Ta=25℃ Note C
V_PWM	PWM Signal Voltage	High	2.0	3.3	3.6	V	-
		Low	0	-	0.5	V	
FPWM	Output PWM frequency		--	200	1K	Hz	-
PWM	PWM Duty ratio		20	-	100	%	-
VLED_EN	LED enable Voltage	High	2.6	3.3	3.6	V	-
		Low	0	-	0.4	V	

A: The LED life time define as the estimated time to 50% degradation of initial luminous.

**B: Strong propose to set LED Input Voltage 5V, it would be best power efficiency.**

C: Calculator value for reference  $PLED = VF(\text{normal Distribution}) \times IF(\text{Normal Distribution}) / \text{Efficiency}$

## 9. Electrical Characteristics

### 9.1 Interface Connector

NO	Symbol	Description	Remark
1	GND	Ground	
2	VDD	Power supply 3.3V (Typ.)	3.0V (Min.) ~3.6V (Max.)
3	VDD		
4	VDD_EDID	Power supply for EDID (3.3V Typ.)	
5	ADJ	System PWM Signal Input	
6	SCL	EDID clock	
7	SDA	EDID Data	
8	RX_O0-	LVDS differential data input	
9	RX_O0+		
10	GND	Ground	
11	RX_O1-	LVDS differential data input	
12	RX_O1+		
13	GND	Ground	
14	RX_O2-	LVDS differential data input	
15	RX_O2+		
16	GND	Ground	
17	RX_OCLK-	LVDS differential clock input	
18	RX_OCLK+		
19	GND	Ground	
20	NC	No connect	
21	NC	No connect	
22	GND_LED	LED Ground	
23	GND_LED		
24	V_LED	LED Power Supply 5V	5.5V (Max.)
25	V_LED		
26	V_LED		
27	NC	No connect	
28	NC	No connect(Reserve)	(TCON SCL,for MJK test)
29	NC	No connect(Reserve)	(TCON SDA,for MJK test)
30	NC	No connect	

Note: All input signals shall be low or Hi-Z state when VDD is off.

# 9.2 LVDS Receiver

## 9.2.1 Signal Electrical Characteristics for LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644 ) standard.

**Table 6 LVDS Receiver Electrical Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
LVDS Input High Threshold	$V_{th}$	-	-	+100	mV	$V_{cm}lvds=1.2V$
LVDS Input Low Threshold	$V_{tl}$	-100	-	-	mV	$V_{cm}lvds=1.2V$
Magnitude Differential Input Voltage	$ V_{id} $	100	-	600	mV	
Common Mode Voltage	$V_{cm}$	1.0	1.2	1.4	V	
Common Mode Voltage Offset	$\Delta V_{cm}$	-	-	50	mV	

**Note:**

- A. Input signals shall be low or Hi-Z state when VDD is
- B. All electrical characteristics for LVDS signal are defined the interface connector of LCD.

Note: All values are at VDD=3.3V, Ta=25 degree C.

**Figure 7 Voltage Definitions**

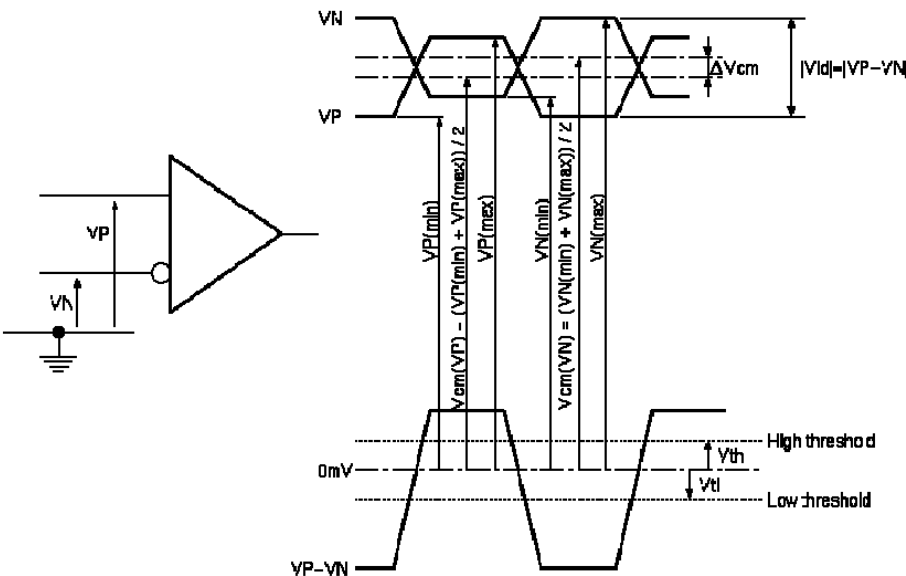


Figure 8 Measurement System

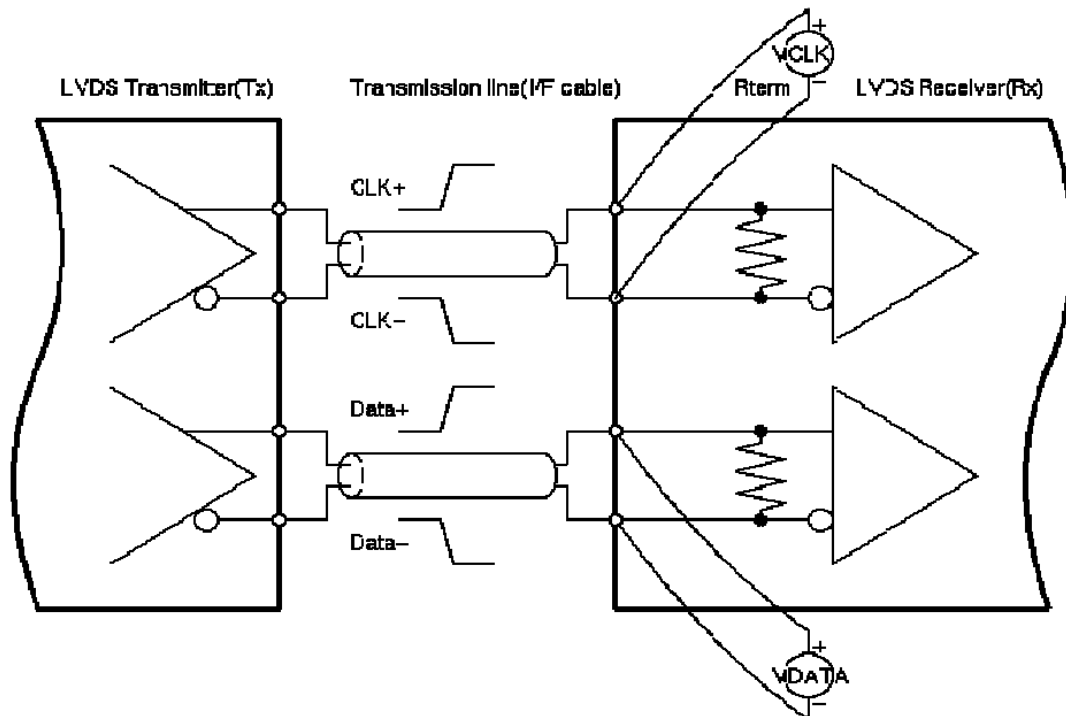
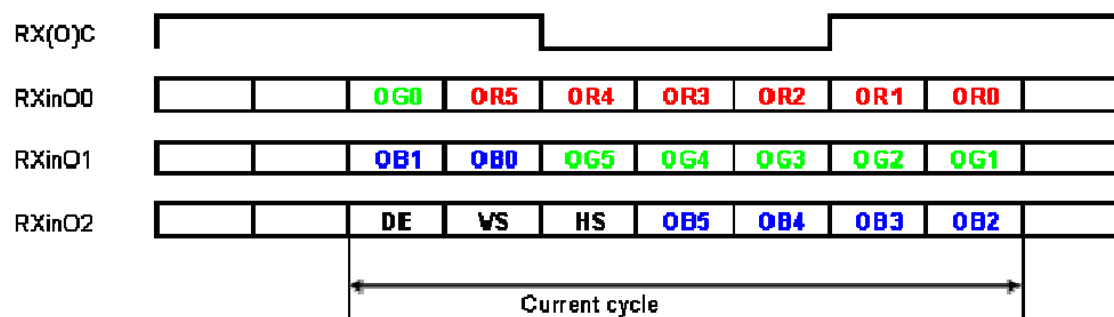


Figure 9 Data mapping

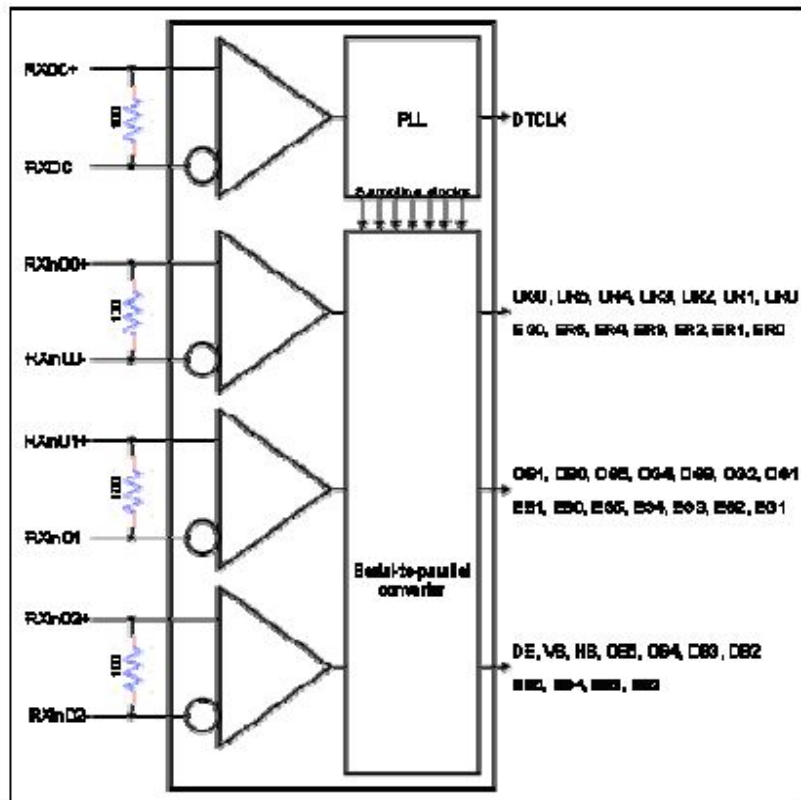




### 9.2.2 LVDS Receiver Internal Circuit

Figure 10 LVDS Receiver Internal Circuit shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Figure 10 LVDS Receiver Internal Circuit



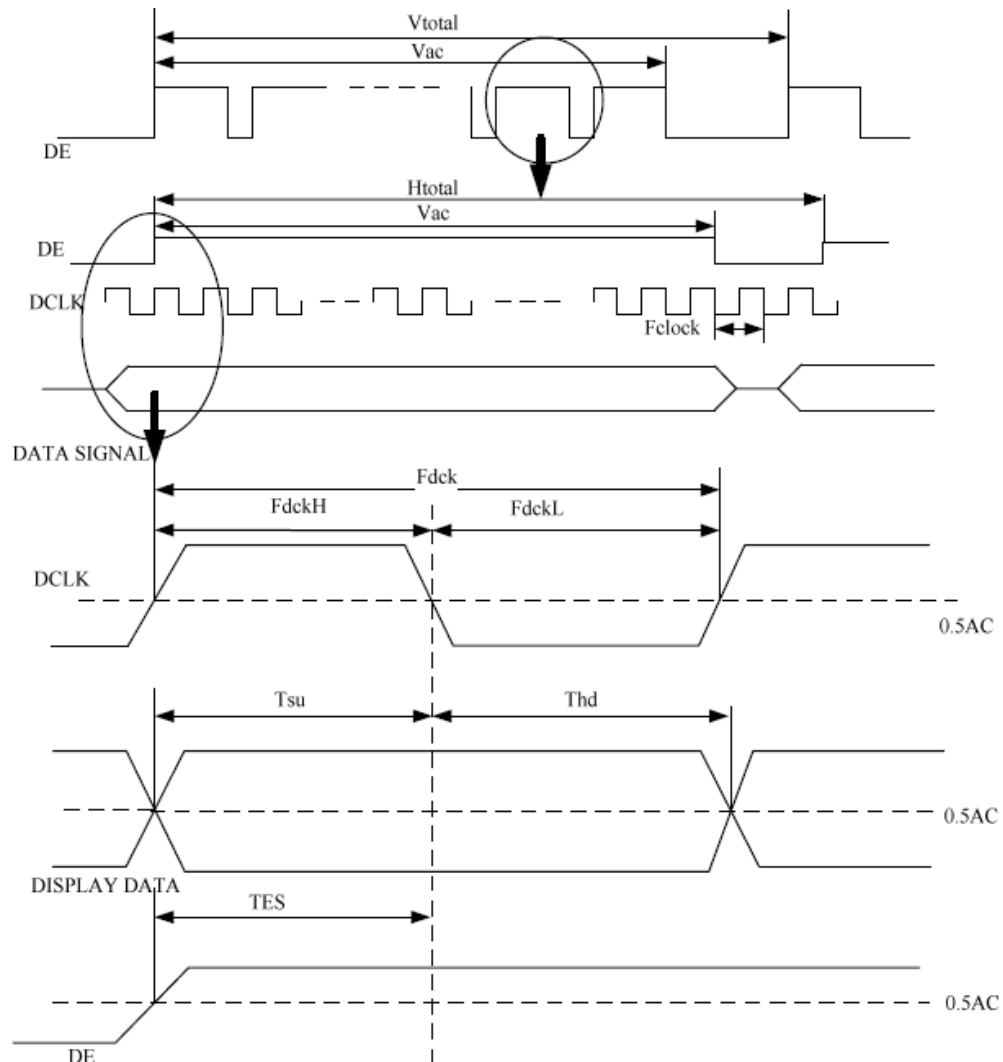
# 10.Interface Timings

## 10.1 Timing Characteristics

**Table 7 Interface Timings**

Parameter	Symbol	Unit	Min.	Typ.	Max.
LVDS Clock Frequency(single)	Fdck	MHz	44.4	50.4	65.2
H Total Time	Htotal	clocks	1320	1344	1362
H Active Time	Hac	clocks	1024	1204	1204
V Total Time	Vtotal	lines	612	625	638
V Active Time	Vac	lines	600	600	600
Frame Rate	Vsync	Hz	55	60	65

**Figure 11 Timing Characteristics**



**Note: TES is data enable signal setup time.**

# 11.Power Consumption

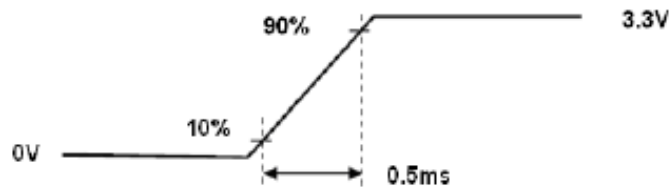
Input power specifications are as follows.

**Table 8 Power Consumption**

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	V	
IDD	VDD Current	--	290	--	mA	All black pattern, 60Hz
PDD	VDD Power	--	0.96	--	W	
Irush	Rush Current	--	--	TBD	A	Note1
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	--	--	300	[mVp-p]	

Note: 1.Measure Condition

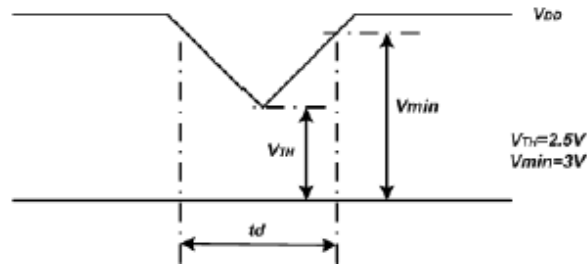
**Figure 12 VDD rising time**



**VDD rising time**

## 2.VDD Power Dip Condition

**Figure 13 VDD Power Dip**

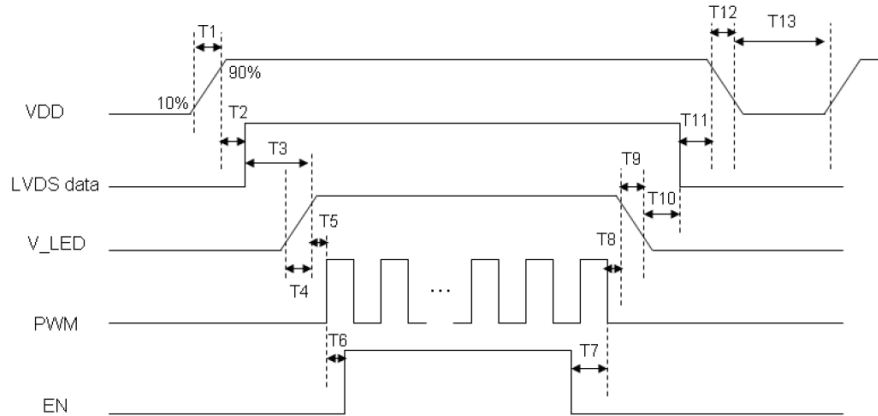


If  $V_{TH} < V_{DD} \leq V_{min}$ , then  $t_d \leq 10ms$ ; when the voltage return to normal our panel must revive automatically.

## 12.Power ON/OFF Sequence

VDD power, interface signals, and lamp on/off sequence are shown in Figure 12. Signals shall be Hi-Z state or low level when VDD is off.

**Figure 12 Power Sequence**



**Table 9 Power Sequencing Requirements**

Parameter	Symbol	Unit	min	typ	max
VDD Rise Time	T1	ms	0.5	--	10
VDD Good to Signal Valid	T2	ms	30		90
Signal Valid to Backlight On	T3	ms	200	--	--
Backlight Power On Time	T4	ms	0.5	--	--
Backlight VDD Good to System PWM On	T5	ms	10	--	--
System PWM ON to Backlight Enable ON(If Have)	T6	ms	--	--	--
Backlight Enable Off to System PWM Off(If Have)	T7	ms	--	--	--
System PWM Off to B/L Power Disable	T8	ms	10	--	--
Backlight Power Off Time	T9	ms	--	10	30
Backlight Off to Signal Disable	T10	ms	200	--	--
Signal Disable to Power Down	T11	ms	0	--	50
VDD Fall Time	T12	ms	--	10	30
Power Off	T13	ms	500	--	--

# 13.Mechanical Characteristics

Figure 13 Reference Outline Drawing (Front Side)

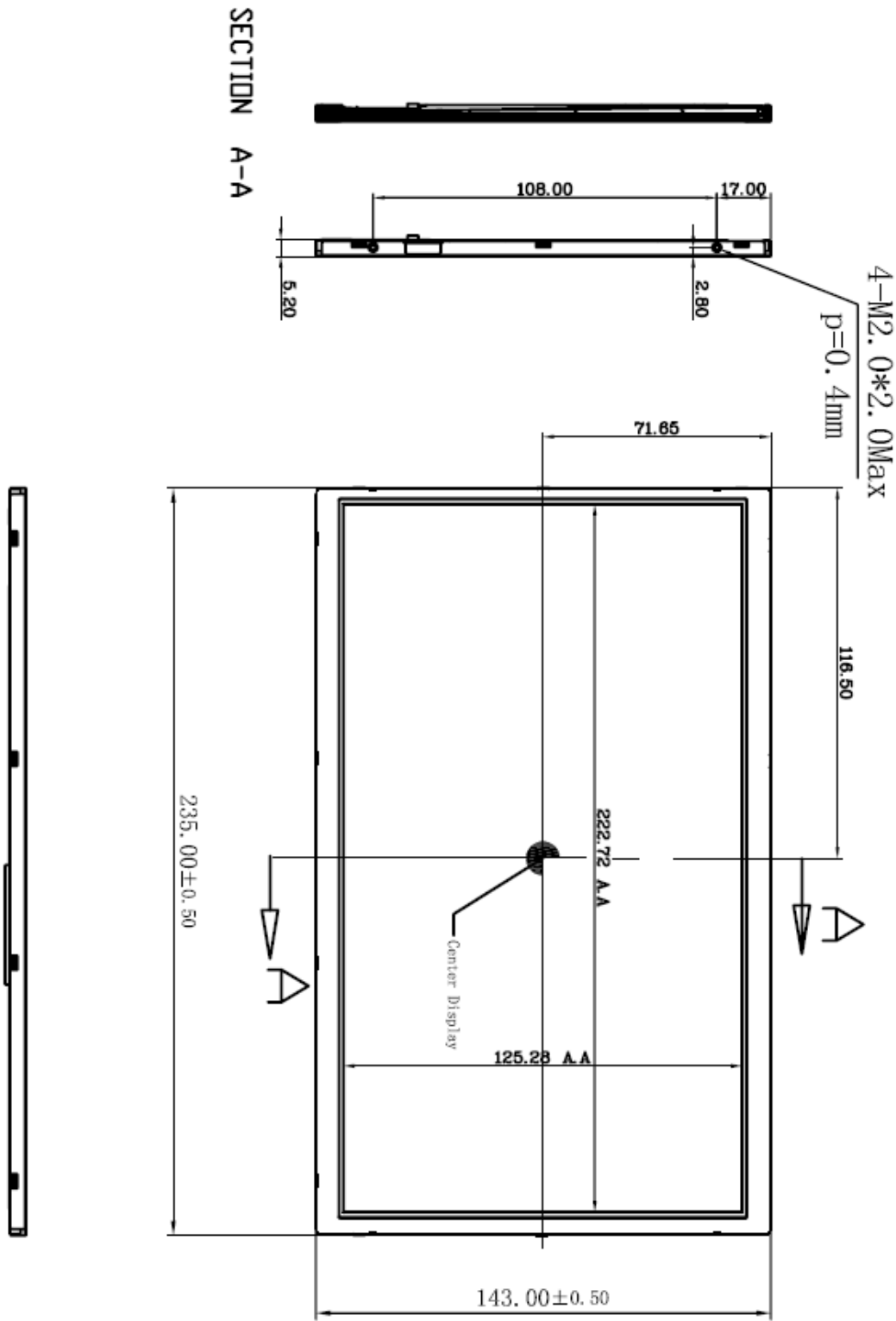
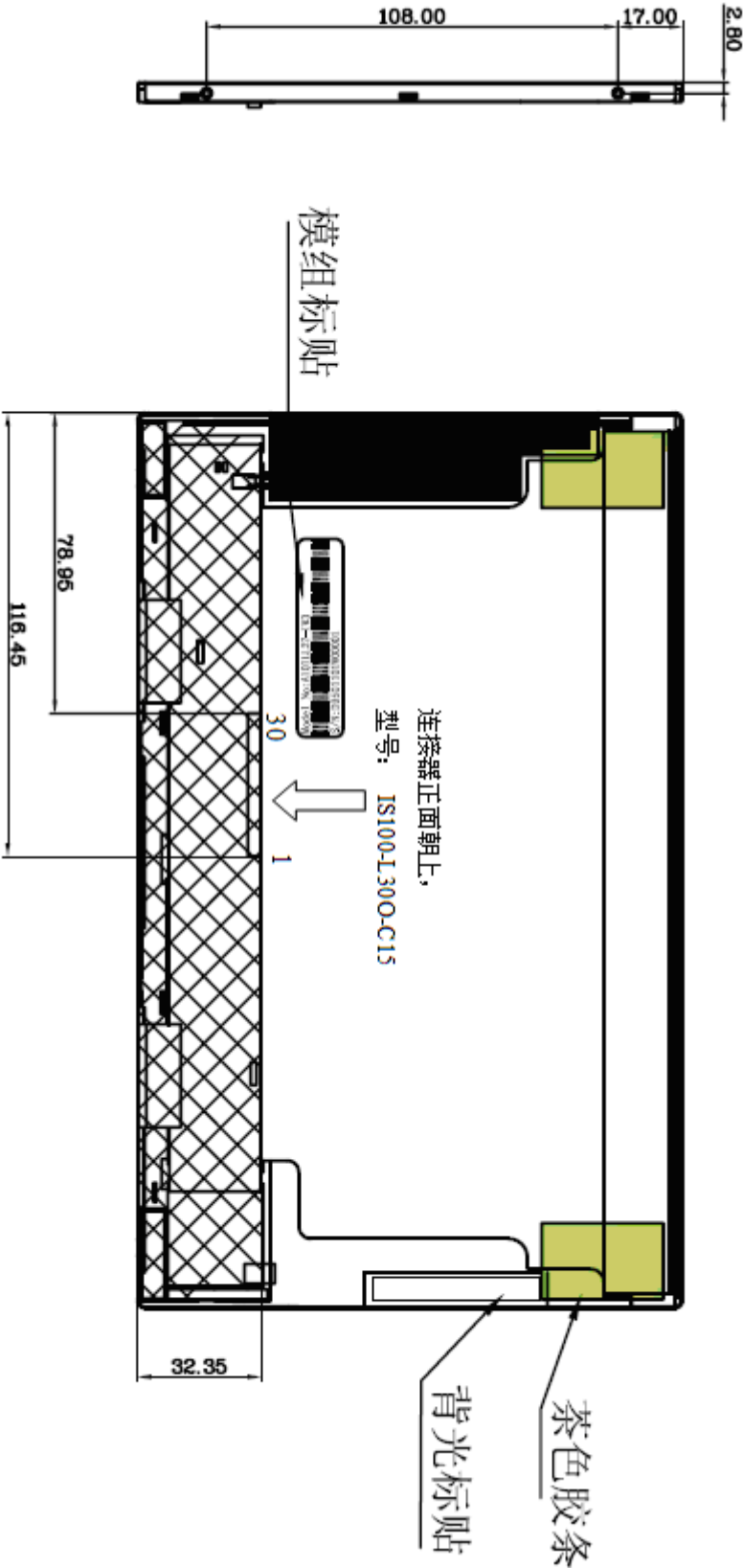


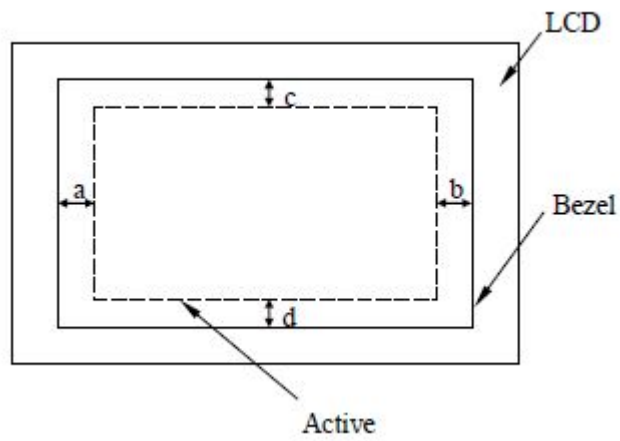
Figure 14 Reference Outline Drawing (Back Side)



### 13.1 Dimension Specifications

**Table 10**

Width(mm)		235.0±0.5
Height(mm)		143.0±0.5
Thickness(mm)		5.2(Typ.),5.4 (max)
Bezel Opening(mm)	X	226.34±0.5
	Y	128.10±0.5
Weight(g)		TBD
BM Width	a,b(mm)	1.81(Typ.)
	c,d(mm)	1.41(Typ.)



## 14. Package

TBD

## 15. EDID Data Structure

Address	Address	Field Name & comments	Value	Value
(Decimal)	(Hex)	FUNCTION	(Hex)	(Binary)
0	0	Header	00	
1	1	Header	FF	
2	2	Header	FF	
3	3	Header	FF	
4	4	Header	FF	
5	5	Header	FF	
6	6	Header	FF	
7	7	Header	00	
8	8	EDID ID manufacturer name ("MJK")	35	
9	9	EDID ID manufacturer name (Compressed ASCII)	4B	
10	0A	Product code	F4	
11	0B	Product code	03	
12	0C	ID S/N (fixed "0")	00	
13	0D	ID S/N (fixed "0")	00	
14	0E	ID S/N (fixed "0")	00	
15	0F	ID S/N (fixed "0")	00	
16	10	Week of manufacture(fixed week code)	1F	
17	11	Year of manufacture(2010 year,fixed year code)	14	
18	12	EDID structure Version # ("1")	01	
19	13	EDID revision # ("3")	03	
20	14	Video I/P definition("digtial")	80	
21	15	Max H image size("222.72mm")	16	
22	16	Max V image size("125.28mm")	0D	
23	17	Display Gamma (Gamma=2.2)	78	
24	18	Feature support(" Active off,RGB Color)	0A	
25	19	Rx1,Rx0,Ry1,Ry0,Gx1, Gx0, Gy1, Gy0	21	
26	1A	Bx1,Bx0,By1,By0,Wx1,Wx0,Wy1,Wy0	D0	
27	1B	Red x(Upper 8 bits)	94	
28	1C	Red y(Higher 8 bits)	58	
29	1D	Green x	56	



30	1E	Green y	8F	
31	1F	Blue x	27	
32	20	Blue y	1F	
33	21	White x	50	
34	22	White y	54	
35	23	Established timings 1(00 if not used)	00	
36	24	Established timings 2(00 if not used)	00	
37	25	Established timings 3(00 if not used)	00	
38	26	Standard timing ID # 1(01 if not used)	01	
39	27	Standard timing ID # 1(01 if not used)	01	
40	28	Standard timing ID # 2(01 if not used)	01	
41	29	Standard timing ID # 2(01 if not used)	01	
42	2A	Standard timing ID # 3(01 if not used)	01	
43	2B	Standard timing ID # 3(01 if not used)	01	
44	2C	Standard timing ID # 4(01 if not used)	01	
45	2D	Standard timing ID # 4(01 if not used)	01	
46	2E	Standard timing ID # 5(01 if not used)	01	
47	2F	Standard timing ID # 5(01 if not used)	01	
48	30	Standard timing ID # 6(01 if not used)	01	
49	31	Standard timing ID # 6(01 if not used)	01	
50	32	Standard timing ID # 7(01 if not used)	01	
51	33	Standard timing ID # 7(01 if not used)	01	
52	34	Standard timing ID # 8(01 if not used)	01	
53	35	Standard timing ID # 8(01 if not used)	01	
54	36	Pixel Clock/10000 LSB{ 50.4MHz)	B0	
55	37	Pixel Clock/10000 USB	13	
56	38	Horz active Lower 8bit	00	
57	39	Horz blanking Lower 8bit	40	
58	3A	HorzAct:HorzBlk Upper 4:4 bit	41	
59	3B	Vertical Active Lower 8bit	58	
60	3C	Vertical blanking Lower 8bit	19	
61	3D	Vert Act:Vert Blk Upper 4:4 bit	20	
62	3E	Horz Sync. Offset	30	
63	3F	Horz Sync. Width	20	
64	40	Vert Sync. Offset:Vert Sync. Width	3A	
65	41	Horz&Vert Sync. Offset/Width Upper 2 bits	00	
66	42	Horizontal Image Size Lower 8 bits	DF	
67	43	Vertical Image Size Lower 8 bits	7D	
68	44	Horizontal and Vertical Image Size Upper 4:4 bit	00	
69	45	Horizontal Border	00	

70	46	Vertical Border	00	
71	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives,	19	
<b>72</b>	<b>48</b>	<b>Detailed timing/Monitor descriptor #2</b>	<b>00</b>	
73	49		00	
74	4A		00	
75	4B	Vendor Defines	0F	
76	4C		00	
77	4D		00	
78	4E		00	
79	4F		00	
80	50		00	
81	51		00	
82	52		00	
83	53		00	
84	54		00	
85	55		00	
86	56		00	
87	57		00	
88	58		00	
89	59	Module revision	01	
<b>90</b>	<b>5A</b>	<b>Detailed timing/Monitor descriptor #3</b>	<b>00</b>	
91	5B	Flag	00	
92	5C	Reserved	00	
93	5D	Defines ASCII string	FE	
94	5E	Flag	00	
95	5F	character of string("")	4D	
96	60	character of string("")	61	
97	61	character of string("")	69	
98	62	character of string("")	4A	
99	63	character of string("")	69	
100	64	character of string("")	4B	
101	65	character of string("")	65	
102	66	New line character indicates end of ASCII string	0A	
103	67	Padding with "Blank" character	20	
104	68	Padding with "Blank" character	20	
105	69	Padding with "Blank" character	20	
106	6A	Padding with "Blank" character	20	
107	6B	Padding with "Blank" character	20	
<b>108</b>	<b>6C</b>	<b>Detailed timing/Monitor descriptor #4</b>	<b>00</b>	

109	6D	Flag	00	
110	6E	Reserved	00	
111	6F	Defines ASCII string	FE	
112	70	Flag	00	
113	71	character of string("M")	4D	
114	72	character of string("D")	44	
115	73	character of string("1")	31	
116	74	character of string("0")	30	
117	75	character of string("1")	31	
118	76	character of string("-")	2D	
119	77	character of string("0")	30	
120	78	character of string("0")	30	
121	79	character of string("9")	39	
122	7A	character of string("-")	2D	
123	7B	character of string("A")	41	
124	7C	New line character indicates end of ASCII string	0A	
125	7D	Padding with “Blank” character	20	
126	7E	Extension Flag	00	
127	7F	Checksum	F2	