



VESA®

Display Data Channel (DDC™) Standard

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DISPLAY DATA CHANNEL STANDARD

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Purpose

The purpose of this standard is to define a communications channel between a computer display and a host system. The channel may be used to carry configuration information to allow optimum use of the display. The channel may also carry display control information. In addition, the channel may be used as a data channel for Access.bus peripherals connected to the host via the display.

Summary

Today's computing environment demands that systems offer user friendly set-up. With the growing popularity of intuitive and simpler software user interfaces, hardware manufacturers are responding with plug-and-play systems and peripherals. However, for the user to receive full benefit from these advances, standardization is necessary. VESA, as the prominent standards organization for graphic sub-systems, has developed a communications channel between the host computer and the display. This communication channel offers basic configuration information plus a standard way of communicating advanced functionality.

Preface

Scope

This revision of the DDC Standard is intended to add support for additional classes of displays as defined in the VESA Plug and Display (P&D) and Flat Panel Display Interface -2 (FPDI-2) standards. It also maintains compatibility with previous revisions of this standard for displays and systems which operate outside the P&D and FPDI-2 standards. To help further clarify unclear areas from previous revisions of the standard an appendix for common questions and answers has been added.

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Revision History

Version 3 December 15, 1997

Addition of DDC Addresses and protocols for P&D and FPDI-2 compatible displays
Addition of compatibility matrix
Removal of DDC2AB and DDC2B+ references from main document into appendix
Clarification of EVC references

Version 2 Revision 1 July 24th 1996

Addition of appendix F to address commonly asked questions
Deletion of section D.2.4 from informative annex D to emphasise that compliance with DDC standard also requires compliance with the I²C specification.
Correction of typographic errors
Correction of references to EDID and DDC standards version and revision levels.

Version 2 Revision 0 April 9th 1996

Clarification of Version 1.0
Requirement to support +5 volts on pin # 9
Addition of application note (appendix D) on implementation of DDC2B and DDC2B+
Addition of DDC2B+ Host System Type
Problems addressed by application notes 1 → 7 inclusive.
Technique to allow display to switch from DDC2 to DDC1 mode
Separation of Extended Display Identification Data (EDID) from the DDC standard - EDID format will be specified in a separate standard
Incorporation of correction and comments arising from VESA membership review of proposal.
The information in this document is identical with the VESA Proposal version 2p revision 0p, dated January 11th 1996.

Version 1.0 Revision 0 August 12, 1994

Initial Standard document
The information in this document is identical with the VESA Proposal version 1.0p, revision 0.64p, dated June 10, 1994

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1. OVERVIEW

1.1 Summary

The Display Data Channel, DDC, described in this document, allows the display to inform the host about its identity and capabilities. The communication channel as used for this purpose is uni-directional from display to host using two different operational modes:

- DDC1 Display data (EDID) is sent continuously, clocked by Vsync
- DDC2B The host system initiates a transfer of the display data record by issuing a request for data to the monitor (EDID and/or VDIF)

The scope of this document is detailed description of these operational modes of DDC and their implementation.

However, in addition to serving this purpose, DDC also allows communication that is bi-directional between the display and host. This enables control of monitor functions affecting the displayed images and possibly use of other devices attached to the I²C bus. Examples of operational modes for this purpose are DDC2AB (ACCESS.Bus) and DDC2B+ modes. These are described in Appendix E and, along with other control protocols, may also be separately documented by VESA. Command sets for these modes will be standardized in the VESA Monitor Control Command Set Standard. As such, description of these modes is outside of the main focus of this document.

This document describes the implementation of the DDC in the standard 15-pin Video Graphic Array (VGA) connector and summarizes the implementation in the VESA Enhanced Video Connector, the VESA Plug & Display Connector and the VESA FPD-2 connector. Other implementations are possible but beyond the current scope of this document.

This document does not specify how the DDC interfaces to the host CPU address and I/O spaces, however, significant consideration has been given to coexistence within current VGA compatible PC systems.

Note : Details of the Extended Display Identification Data (EDID) and Video Display Identification File (VDIF) formats that may be carried by the DDC are beyond the scope of this document. The VESA EDID and / or VESA VDIF standards should be referenced..

1.2 Background

Earlier monitor identification schemes are only capable of handling a limited number of display types and parameters. Since these schemes carry no information about the capabilities of the display, they are of limited value.

Earlier versions of DDC and EDID defined a communication method and configuration data appropriate for traditional CRT displays, but limited in their support of other display types. As these displays types are being defined and standardized by VESA through the P&D and FPD-2 standards, support for communication methods and configuration information suitable for these display is a requirement.

1.3 Standard Objectives

The DDC was developed by VESA to meet, exceed and / or complement certain criteria. These criteria are set forth as Standard Objectives as follows :

- Support Microsoft® Plug and Play definition
- Provide information to allow the graphic sub-system to be configured based on the capabilities of the attached display
- Ensure scaleable, low cost, fast market acceptance
- Allow for base level to be achieved with minimal hardware cost penalties in host controller and display

- Retain compatibility with most existing graphic controller chips at minimum configuration level
- Define a full communication channel capable of sending both EDID and VDIF files, and carrying signals to / from other I/O devices such as keyboard and mouse as well as allowing control of display parameters from the host.

1.4 Reference Documents

Note : Versions identified here are current but user's of this standard are advised to ensure they have the latest versions of reference standards and documents.

- VESA, Video Display Identification Format - VDIF - Standard, Version 1.0.
- VESA, Display Power Management Signaling - DPMS - Standard, Version 1.0.
- VESA, Video BIOS Extensions For Display Data Channel - VBE/DDC - Standard.
- VESA, Extended Display Identification data Standard - EDID - Standard, Version 2, Revision 0
- VESA, Extended Display Identification data Standard - EDID - Standard, Version 3, Revision 0
- VESA, Enhanced Video Connector Standard - EVC - Standard, Version 1
- VESA Plug and Display Standard - P&D - Standard, Version 1
- VESA Flat Panel Display Interface-2 (FPDI-2) (Currently proposed)
- VESA Monitor Control Command Set (Currently proposed)
- Access.bus Monitor Command Set - Section 7 of Access Bus Specification V3.0
- Philips I²C bus specification - Data Handbook I²C Peripherals for Microcontrollers 1/92.
- Access.bus Specification, Version 3.0
- Microsoft / Intel Plug and Play ISA Specification, Version 1.0, May 28th 1993.
- Microsoft / Intel Plug and Play Errata and Clarification Document, 12/10/93.
- IBM Personal System/2 Hardware Interface Technical Reference- Common Interfaces Video Subsystem

1.5 Compatibility with Non-DDC System Units / Graphic Cards

Several older graphic sub-systems and boards which use the ID bits to identify the attached monitor type may have a problem with a DDC monitor since ID bits 1 has been redefined and may be read as either a '1' or '0' dependent on when it is read.

Use of one of the following options should be considered to avoid this problem :

- Avoid compatibility claims for these systems and boards
- Clearly label monitor as suitable for DDC capable graphic sub-systems and boards only
- Provide or recommend a pass-through connector which isolates the monitor DDC lines from the graphic sub-system or board
- Implement a switch (hardware or software) to allow user to disable the monitor DDC function

1.6 Compatibility with previous DDC implementations

Systems compatible with previous versions of DDC may not be compatible with parts of this version designed to support display for the Plug & Display and FPDI-2 standards. In many cases these displays are not designed to operate with the older systems. In other cases where the P&D or FPDI compatible display can also operate with these older systems it is recommended that the display continue to implement DDC version 2 revision 0 in addition to the DDC requirements of P&D or FPDI-2.

Systems designed for the Plug & Display standard may have some level of compatibility with existing monitors which are not directly designed for P&D. It is recommended, therefore, that system designs continue to provide support for DDC2B as defined in DDC standard version 2.0 to support these monitors.

2. DEFINITIONS

2.1 File formats

2.1.1 Extended Display Identification Data : EDID

Data structure containing the display identity and the basic display specifications. Two versions of the data structure are defined. Version 1 is a 128-byte structure. Version 2 is a 256-byte structure. Details in VESA EDID standard

2.1.2 Video Display Identification Format : VDIF

A data structure containing the full display specification. Details in VESA VDIF standard.

2.2 Communication Protocols

2.2.1 I²C Bus

A standard protocol 2-wire (clock and data) serial data bus. See I²C standard for details.

2.2.2 Access.bus

A standard protocol which defines standard messages for initialization, device identification, address assignment (configuration process) for device specific reports and control information. Details are in the ACCESS.bus specification..

2.3 Communications Channel Type

2.3.1 DDC1

A uni-directional data channel from the display to the host which carries continuous transmission of the EDID information.

Note: DDC1 can only be used to transmit EDID Version 1 data structure.

2.3.2 DDC2

A bi-directional data channel between the display and host based on I²C protocol. In DDC2B mode the only transmission from the host to the monitor is a request for either EDID or VDIF data but in DDC2 monitor control modes a true bi-directional communications exists with data being transferred from the monitor to the system plus commands being sent from the system to the monitor to adjust the monitor front of screen appearance. In addition, the DDC2AB channel can act as a transparent channel for ACCESS.bus communication.

2.4 Display/Host Communication Channels

2.4.1 DDC1 Communications

DDC1 is a uni-directional channel from display to host. Display data is sent continuously to the host system, clocked by Vsync.

2.4.2 DDC2B Communications

DDC2B is a uni-directional channel from display to host The host initiates the data transfer by reading the EDID and/or VDIF information from an I²C slave memory location. Various memory locations are defined to support different EDID structures and different types of devices

2.5 Display Type

2.5.1 Old Display

Older type displays with no DDC capability.

2.5.2 DDC1/2B Display

Displays capable of continuously transmitting EDID data using DDC1 communication channel.

In addition, the display is capable of detecting and responding to a request for EDID or VDIF format data transmitted via DDC2B communication channel. A display detecting a DDC2B capable host shall switch to DDC2B communications.

2.5.3 DDC1/2AB Display

Displays capable of extensions beyond DDC1 and DDC2B. This type of display is considered an ACCESS.bus device, EDID or VDIF data can be read using either DDC2B or ACCESS.bus commands. Additional ACCESS.bus commands (beyond retrieval of EDID and / or VDIF data) to the display may be supported. A display detecting a DDC2 capable host shall switch to DDC2 communications.

2.5.4 P&D/FPDI-2 Display

Displays which conform to the VESA Plug and Display standard or the VESA FPDI-2 standard do not incorporate DDC1 mode. In host systems which address these displays, DDC1 is not used.

2.6 Host System Type

2.6.1 Old Host

Older type systems with no DDC capabilities.

2.6.2 DDC1 Host

Systems capable of reading the DDC1 data stream.

2.6.3 DDC2B Host (A0 addressing)

Systems capable of communicating with the display using DDC2B commands. This host is designed to address only the original I²C location for DDC (A0h).

2.6.4 P&D Host (Ax addressing)

Systems capable of communicating with the display using DDC2B commands. This host is capable of addressing P&D designated I²C addresses (A2 and A4) in addition to the original A0h address location

2.6.5 FPDI-2 Host (Ax addressing)

Systems capable of communicating with the display using DDC2B commands. This host is capable of addressing FPDI designated I²C addresses (A6 & A8).

2.7 DDC System/Display Matrix

The matrix in Table 2.1 shows interoperability of DDC operation between monitors and systems of different types. For each case where interoperability is possible, the matrix shows the EDID block size, the DDC mode used and the DDC address where the data is found.

	Legacy Monitor	DDC ver 1 or 2 compatible Monitor	P&D-D Monitor	DDC monitor with EDID data structure ver 2 (256 byte)	Integrated Flat Panel w/DDC
Host without DDC capabilities	No DDC	No DDC	N/A	No DDC	N/A
DDC1 capable Host system	No DDC	128-byte EDID in DDC1 mode	N/A	128-byte EDID in DDC1 mode	No DDC
DDC2 capable host compatible with DDC Ver.2 Standard	No DDC	128-byte EDID in DDC2B mode at address A0h	N/A	128-byte EDID in DDC2B mode at address A0h	No DDC
DDC2 capable host compatible with DDC Ver.3 Standard	No DDC	128-byte EDID in DDC2B mode at address A0h	256-byte EDID in DDC2B mode at address A2h	256 byte EDID in DDC2B mode at address A2h	256-byte EDID in DDC2B mode at address A6h

Table 2.1 - DDC System/Display Matrix

3. DDC Version 2.0 Compliant System/Monitor Combinations

3.1 COMMUNICATION PROTOCOL

There are two forms of communication protocol. In both, display capabilities are retrieved by the system software during the boot-up and configuration time. The retrieved data provides the system unit information about the attached display capabilities.

There is no standard definition of how the DDC signals are interfaced to the host CPU memory or I/O space. It is envisioned that each hardware manufacturer will provide the software necessary to transfer the EDID or VDIIF information to the operating system. For the PC platform, this software layer is defined in the VESA BIOS Extension / Display Data Channel, VBE/DDC, standard.

3.1.1 DDC1 Overview

DDC1 is a uni-directional data channel from the display to the host allowing for continuous transmission of the EDID data only.

3.1.2 DDC2 Overview

Note : Successful DDC operation requires that all designs implement the requirements of the I²C and ACCESS.bus specifications (as appropriate). Design not implementing these requirements shall not be considered compliant with the VESA DDC Standard.

3.1.2.1 Normal Operation

DDC2 is a bi-directional data channel between the display and host based on the I²C bus. Within DDC2 there are two types of protocols defined.

- DDC2B - A simple protocol to read in I²C memory data.
- DDC2 monitor control protocols - I²C based protocols with various levels of complexity which operate over the DDC channel for the purpose of controlling the monitor.

A display detecting a DDC2 capable host, will automatically switch to DDC2 operation. The display can detect a DDC2 capable host by sensing I²C activity.

In a system capable of DDC2 monitor control protocols the host determines if the display is also capable of these protocols by trying to establish contact. If contact is not established, then the host should revert to the simpler DDC2B protocol and read the I²C memory location to retrieve EDID or VDIIF data.

3.1.2.2 Error Recovery

Note : Provision of this recovery mechanism is optional but **strongly** recommended for new designs of DDC1/DDC2 displays.

When a display first switches to DDC2 it enters an interim state which is functionally identical to DDC2 operation but if the transaction is not completed within either 128 Vsync periods or a period of approximately 2 seconds then it shall revert to DDC1 mode.

Successful completion of the transaction within 128 Vsync periods or within the 2 second period shall cause the display to enter the normal DDC2 state.

See Section 4.1.1 for additional details.

3.2 DDC LEVEL SELECTION

3.2.1 Display

A display shall be DDC1 and DDC2 capable, with DDC2 having the higher priority. The display shall start transmitting DDC1 data whenever it is powered on and a vertical synchronization signal is detected from the host. The display shall switch to DDC2 as soon as it sees a high to low transition on the clock line (SCL) indicating that there are other DDC2 devices connected to the bus. This procedure will cause a transmission error, however, both the display and host shall have error detection and a method to recover from temporary transmission errors. Once the display switches from DDC1 to DDC2 mode it shall remain in DDC2 mode for the duration of that power-on period, except where the optional error recovery mode (see below) is implemented.

3.2.1.1 *Optional Error Recovery Mode*

Provision of this recovery mechanism is optional but **strongly** recommended for new designs.

The display shall have a transition state on entry to DDC2 mode from which it can revert to DDC1 mode if it receives 128 vertical sync. pulses (Vsync) while the SCL line is idle (see note 1). If the monitor sees a valid DDC2 control byte, it will lock into DDC2 and thereafter disregard Vsync. When in the transition state, the count of vertical sync pulses shall be reset by any activity on the SCL line (see note 2). The purpose of this option is to allow for recovery of a system with a DDC1 host in which spurious noise causes the display to enter DDC2 mode.

Note 1 : Use of a counter is one possible implementation, it is also acceptable to use a timer to achieve the same purpose and this may be a more acceptable implementation, particularly in designs utilizing microprocessors. For convenience ‘timer’ will be used in this document to indicate this function regardless of actual implementation method.

Note 2 : Regardless of implementation details, intent is to return to DDC1 mode after approximately two seconds unless there is SCL line activity when counter or timer will be reset or a valid DDC2 control byte is received when the monitor will lock into DDC2.

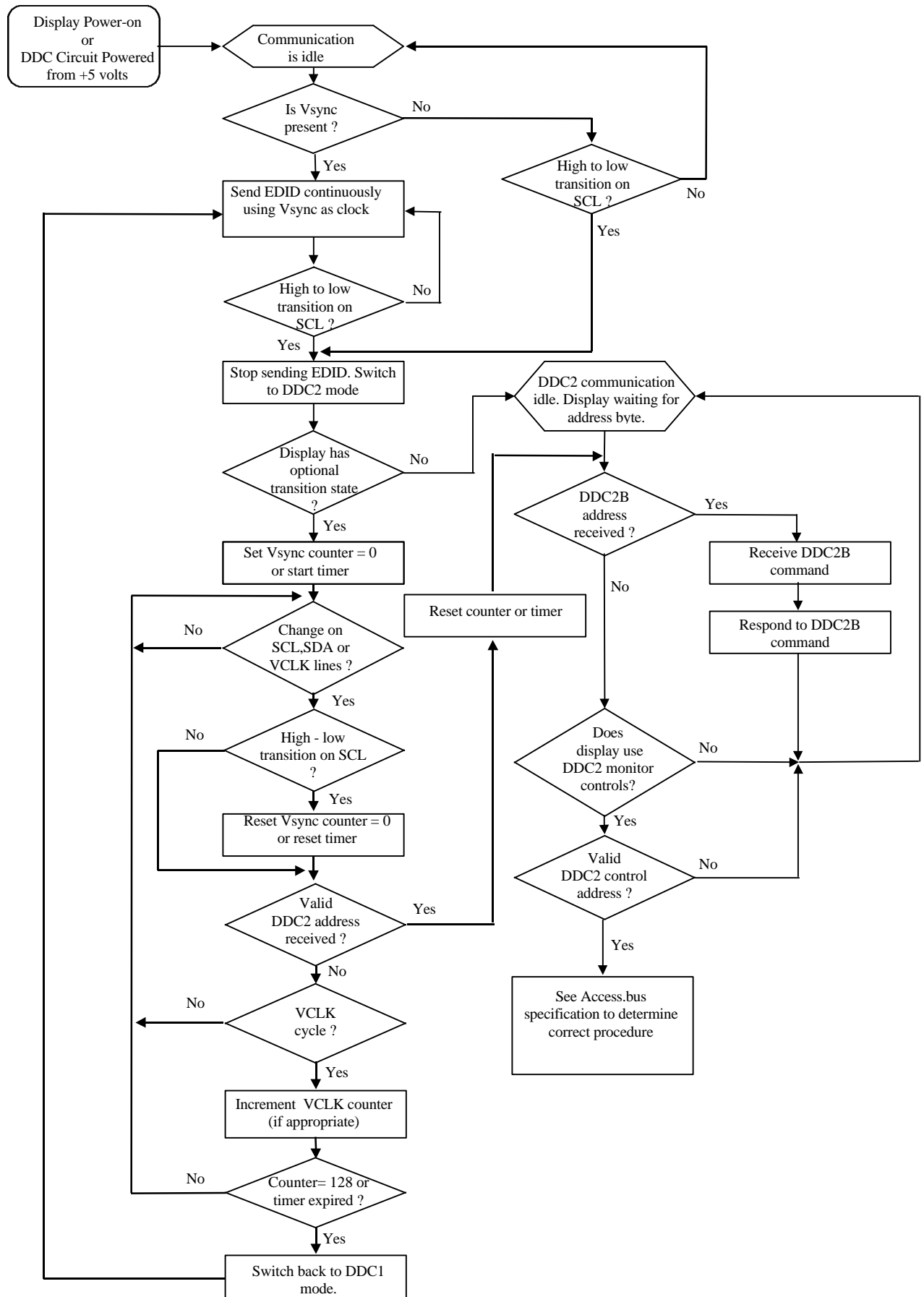
Note 3 : Implementing this option in the display does not remove the need for good design practice to minimize the probability of noise on the SCL line causing the display to erroneously enter DDC2 mode.

3.2.1.2 *DDC Operation Level Selection : Display View Flow Chart*

The following flow chart is provided for guidance purposes only, the text description of DDC operation takes precedence.

Notes

- If the display does not support the optional transition state then, once the monitor has switched to DDC2 mode, it will remain in DDC2 mode for the duration of that power-on period.
- If the display has the optional transition state then this state shall have all of the DDC2 capabilities. The display shall be able to respond to the first valid control byte.
- For details of DDC2B to DDC2AB and DDC2B to DDC2B+ mode changes and ACCESS.bus operation, refer to the Appendix E and the ACCESS.bus monitor device protocol specification.



3.2.2 Host System

3.2.2.1 DDC1 Capable Host

A DDC1 capable host shall try to read the DDC1 data stream sent by the display. If repeated errors are detected, then the host shall decide that the display is of type “Old” and incapable of DDC operation.

In this case, the display ID lines may be read according to earlier industry practice.

Note: A host system designed for compliance with the Plug and Display or FPD-2 standards cannot be a DDC1 type host

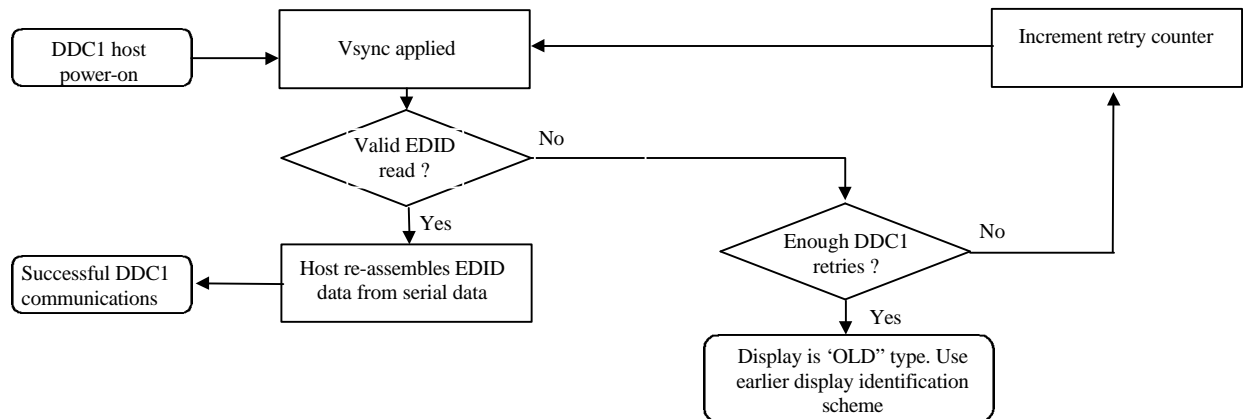
3.2.2.2 DDC2B Capable Host

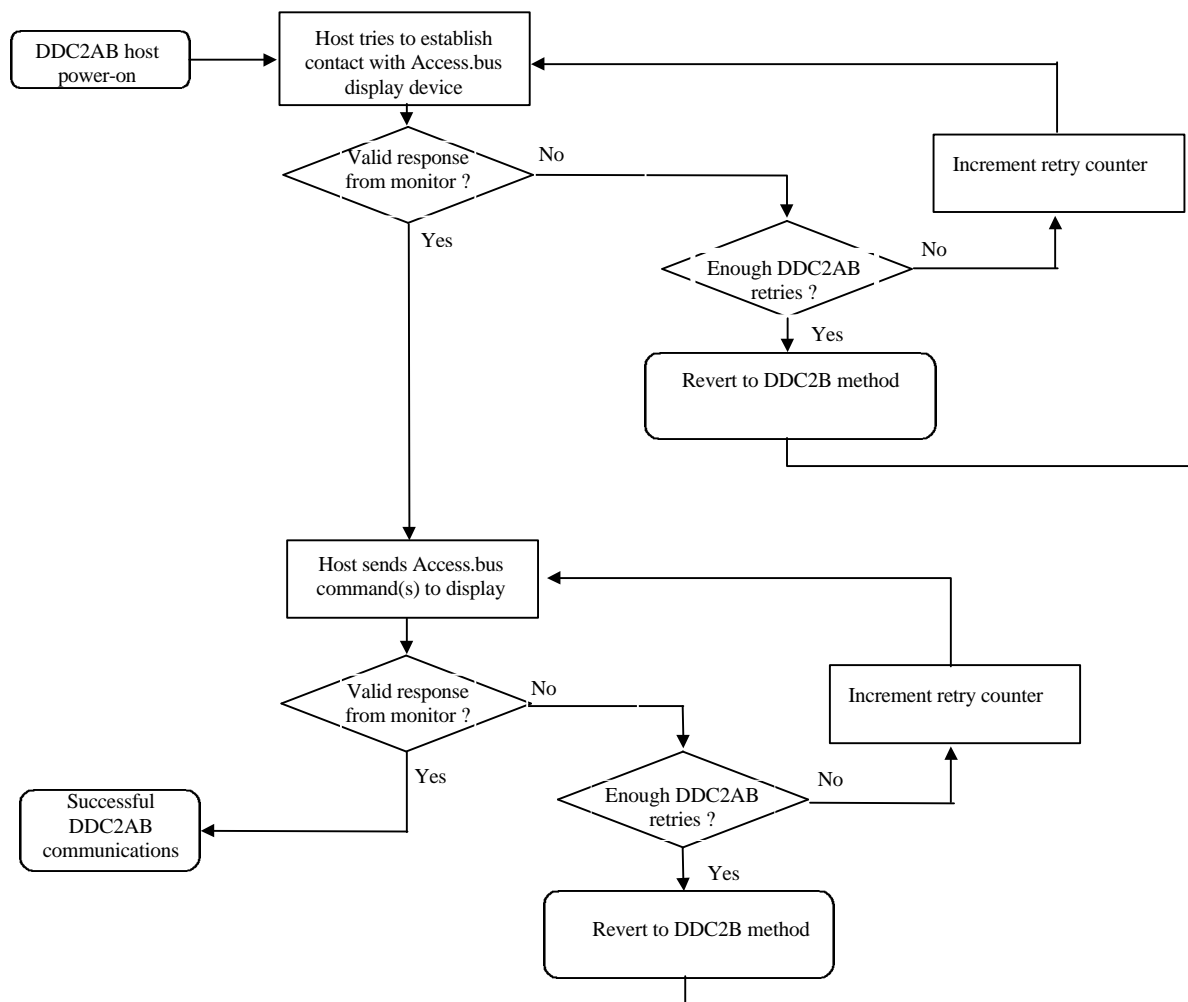
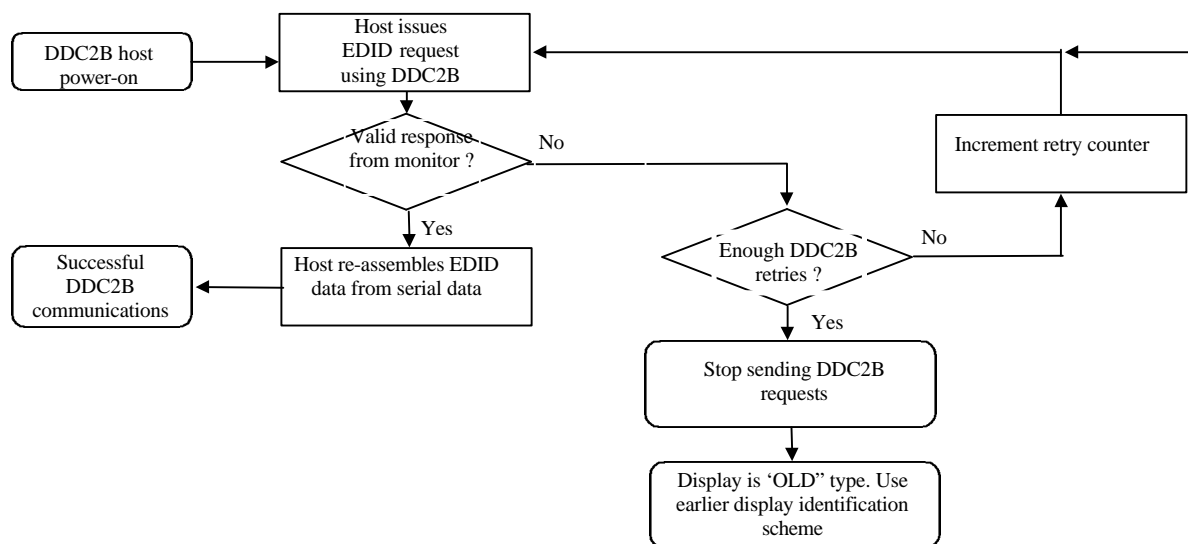
The DDC2B system should issue a request for the EDID data using DDC2B protocol. If the host is P&D or FPD-2 capable, the request should be made to the P&D or FPD-2 defined I2C address location. If no valid response is received or the host is not P&D or FPD-2 capable, the host shall issue a request for EDID data using DDC2B protocol at the default DDC I2C location of A0h. If no valid response is received then the host shall stop sending DDC2B requests to the display and assume that the display is of type “Old”.

Note: At least one retry should be attempted before reaching a decision.

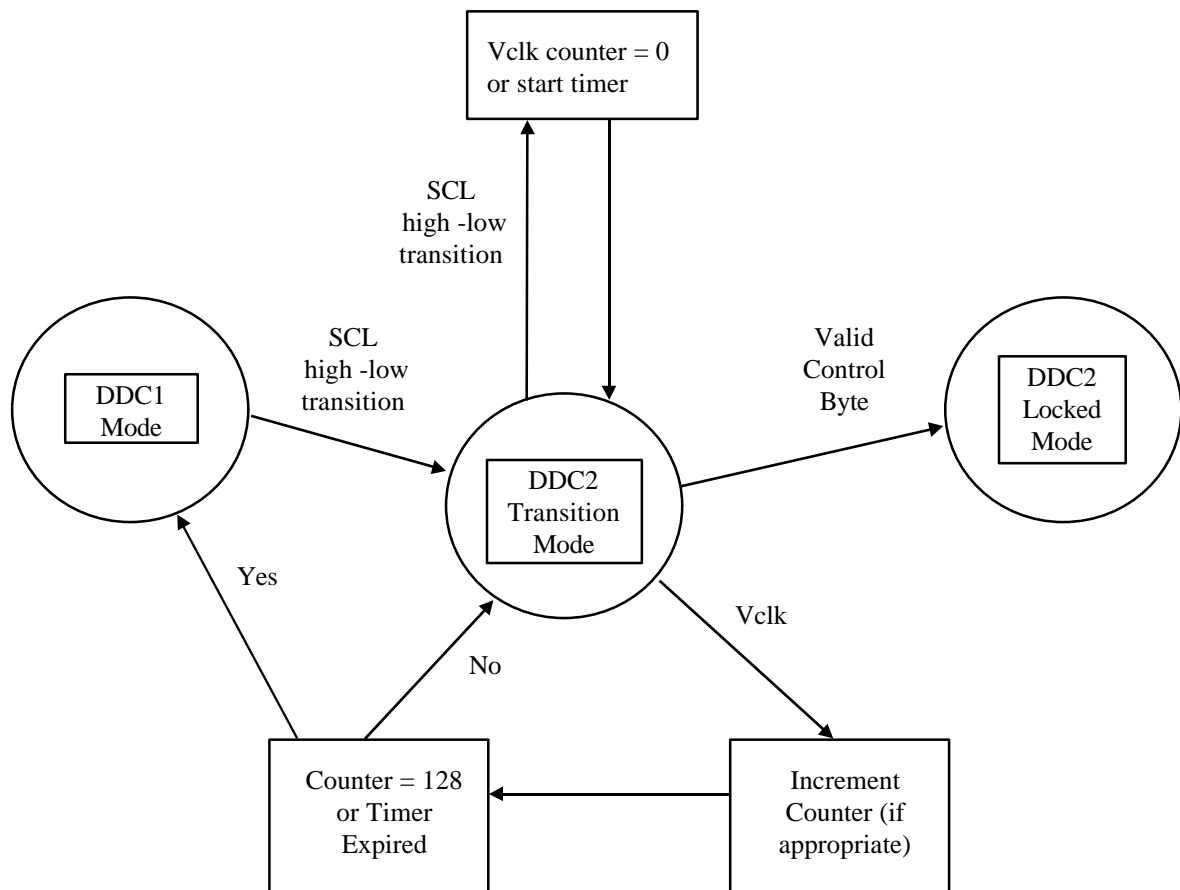
3.2.2.3 DDC Operation Level Selection : Host View Flow Charts

Note : In order to respond the display DDC circuit must have power - supplied either from the monitor or by + 5 volts on socket # 9 (VGA connector) or pin # 28 (EVC connector) from the system. It is recommended that new monitor designs use the +5 volts supplied by the host.





3.2.2.4 State diagram of DDC monitor :



4. P&D Compliant Host/Monitor Combinations

4.1 COMMUNICATION PROTOCOL

Display capabilities are retrieved by the system software during the boot-up and configuration time. The retrieved data provides the system unit information about the attached display capabilities.

There is no standard definition of how the DDC signals are interfaced to the host CPU memory or I/O space. It is envisioned that each hardware manufacturer will provide the software necessary to transfer the EDID information to the operating system. For the PC platform, this software layer is defined in the VESA BIOS Extension / Display Data Channel, VBE/DDC, standard.

Host systems compliant with P&D use DDC2 protocols to read EDID from the display

4.1.1 DDC2 Overview

Note: Successful DDC operation requires that all designs implement the requirements of the I²C and ACCESS.bus specifications (as appropriate). Design not implementing these requirements shall not be considered compliant with the VESA DDC Standard.

4.1.1.1 Normal Operation

DDC2 is a bi-directional data channel between the display and host based on the I²C bus. Within DDC2 there are two types of protocols defined.

- DDC2B - A simple protocol to read in I²C memory data.
- DDC2 monitor control protocols - I²C based protocols with various levels of complexity which operate over the DDC channel for the purpose of controlling the monitor.

A display detecting a DDC2 capable host, will automatically switch to DDC2 operation. The display can detect a DDC2 capable host by sensing I²C activity.

In a system capable of DDC2 monitor control protocols the host determines if the display is also capable of these protocols by trying to establish contact. If contact is not established, then the host should revert to the simpler DDC2B protocol and read the I²C memory location to retrieve EDID or VDIF data.

4.2 DDC LEVEL SELECTION

4.2.1 Display

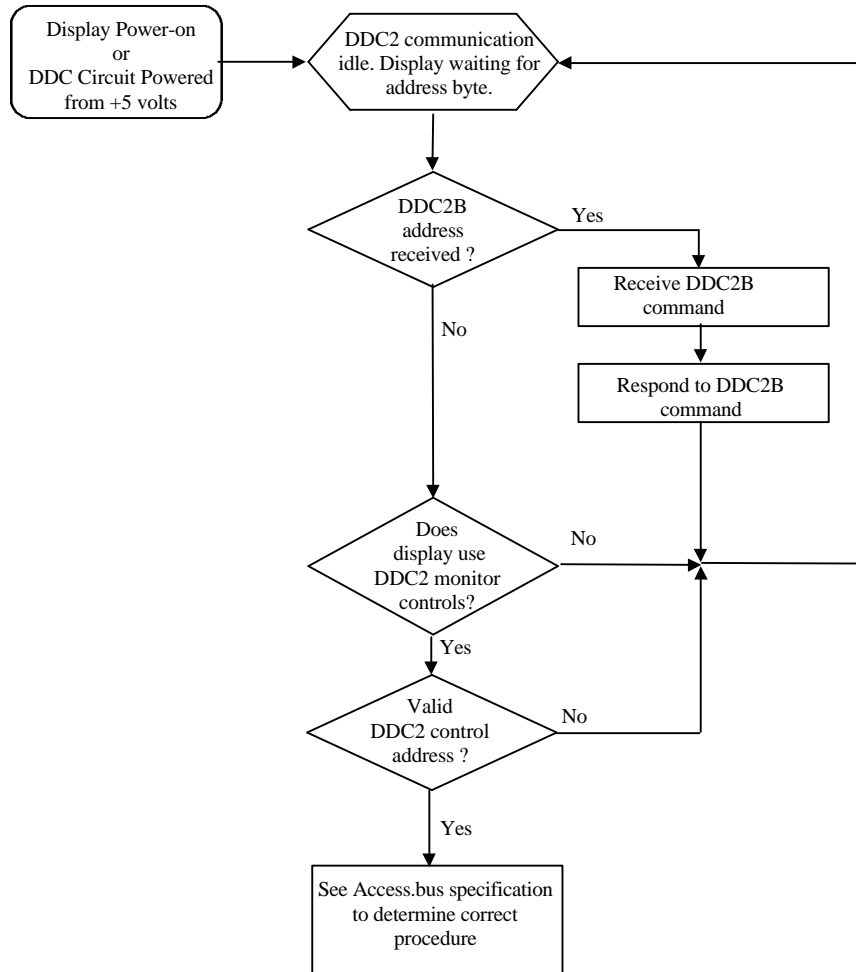
A P&D display shall be DDC2 capable. If the display is not backward compatible with EVC Standard version 1 or earlier versions of DDC, and does not supply EDID at the A0h I2C address, support of DDC1 is not necessary and the display is always in DDC2 mode.

If in addition to supporting P&D, the display desires backward compatibility with the EVC Version 1 standard and supplies EDID at the A0h I2C address, the display shall be both DDC1 and DDC2 capable with DDC2 having the higher priority. In this case DDC level selection is the same as described in Section 3.2.1 of this document.

4.2.1.1 DDC Operation Level Selection : Display View Flow Chart

The following flow chart is for guidance only, the text description of DDC operation takes precedence.

Note: For details of DDC2B to DDC2AB and DDC2B to DDC2B+ mode changes and ACCESS.bus operation, refer to Appendix E and the ACCESS.bus monitor device protocol specification.



4.2.2 Host System

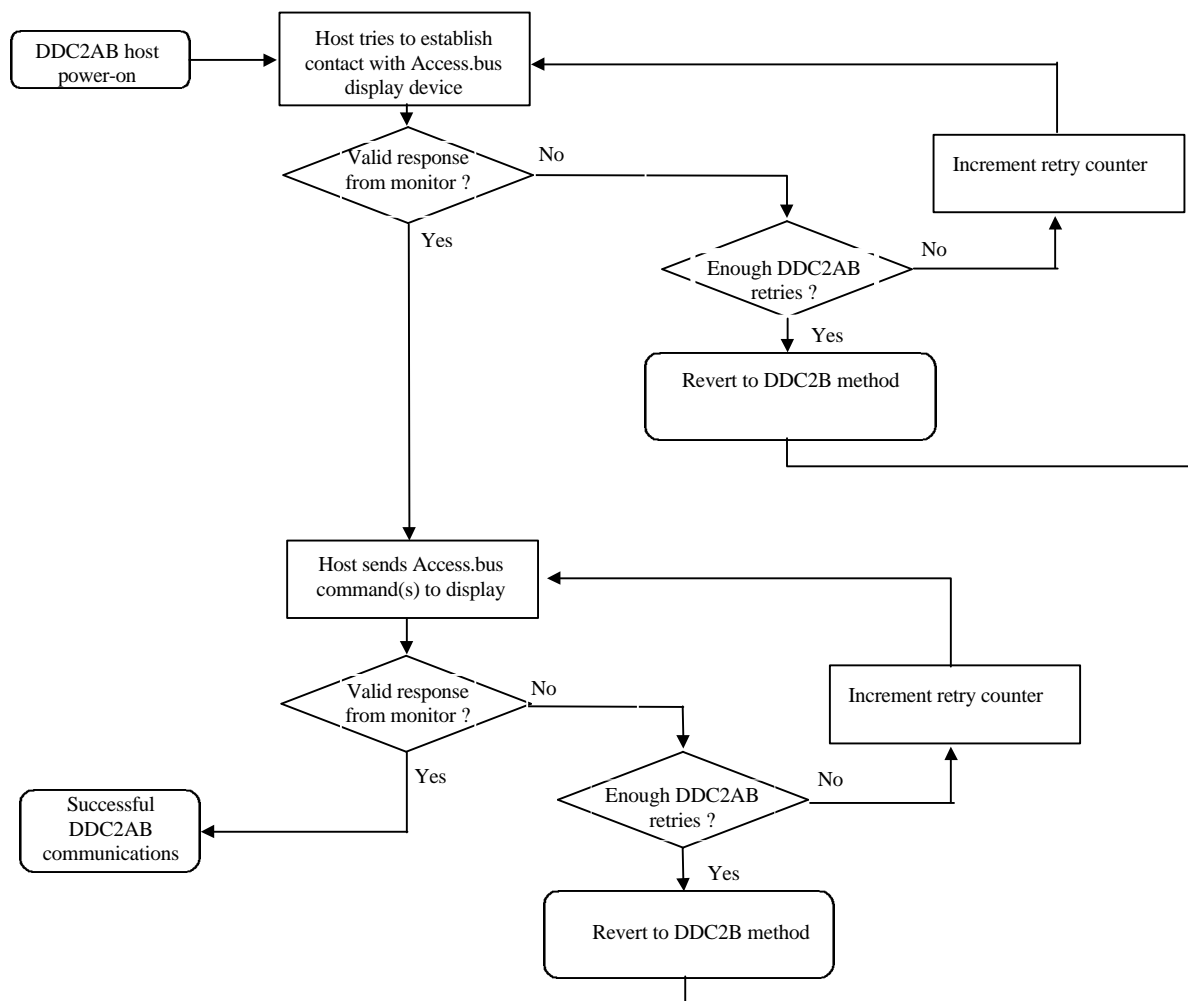
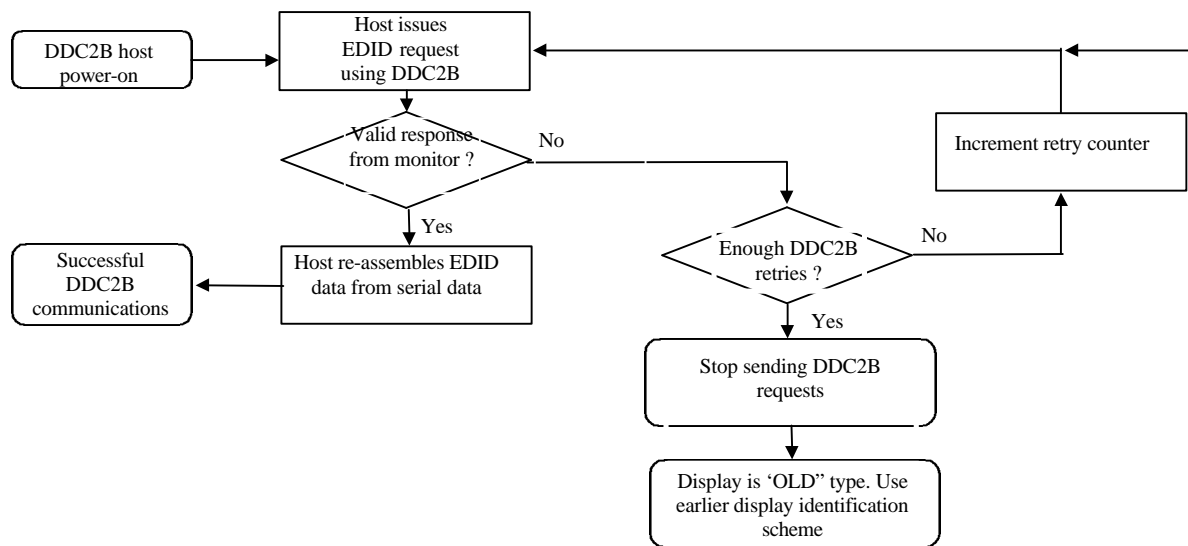
4.2.2.1 DDC2B Capable Host

The DDC2B system should issue a request for the EDID data using DDC2B protocol, to the P&D defined I2C address location. If no valid response is received the host shall issue a request for EDID data using DDC2B protocol at the default DDC I2C location of A0h. If no valid response is received then the host shall stop sending DDC2B requests to the display and assume that the display is of type “Old”.

Note : At least one retry should be attempted before reaching a decision.

4.2.2.2 DDC Operation Level Selection : Host View Flow Charts

Note : In order to respond the display DDC circuit must have power - supplied either from the monitor or by + 5 volts on pin # 28 (P&D or EVC connector) from the system. It is recommended that new monitor designs use the +5 volts supplied by the host.



5. FPD-2 Compliant Graphics Controller/Display Combinations

5.1 COMMUNICATION PROTOCOL

Display capabilities are retrieved by the system software during the boot-up and configuration time. The retrieved data provides the system unit information about the attached display capabilities.

There is no standard definition of how the DDC signals are interfaced to the host CPU memory or I/O space. It is envisioned that each hardware manufacturer will provide the software necessary to transfer the EDID information to the operating system. For the PC platform, this software layer is defined in the VESA BIOS Extension / Display Data Channel, VBE/DDC, standard.

Host systems compliant with FPD-2 use DDC2 protocols to read EDID from the display

5.1.1 DDC2 Overview

Note: Successful DDC operation requires that all designs implement the requirements of the I²C and ACCESS.bus specifications (as appropriate). Design not implementing these requirements shall not be considered compliant with the VESA DDC Standard.

5.1.1.1 Normal Operation

DDC2 is a bi-directional data channel between the display and host based on the I²C bus. Within DDC2 there are two types of protocols defined.

- DDC2B - A simple protocol to read in I²C memory data.
- DDC2 monitor control protocols - I²C based protocols with various levels of complexity which operate over the DDC channel for the purpose of controlling the monitor.

A display detecting a DDC2 capable host, will automatically switch to DDC2 operation. The display can detect a DDC2 capable host by sensing I²C activity.

In a system capable of DDC2 monitor control protocols the host determines if the display is also capable of these protocols by trying to establish contact. If contact is not established, then the host should revert to the simpler DDC2B protocol and read the I²C memory location to retrieve EDID or VDIF data.

5.2 DDC LEVEL SELECTION

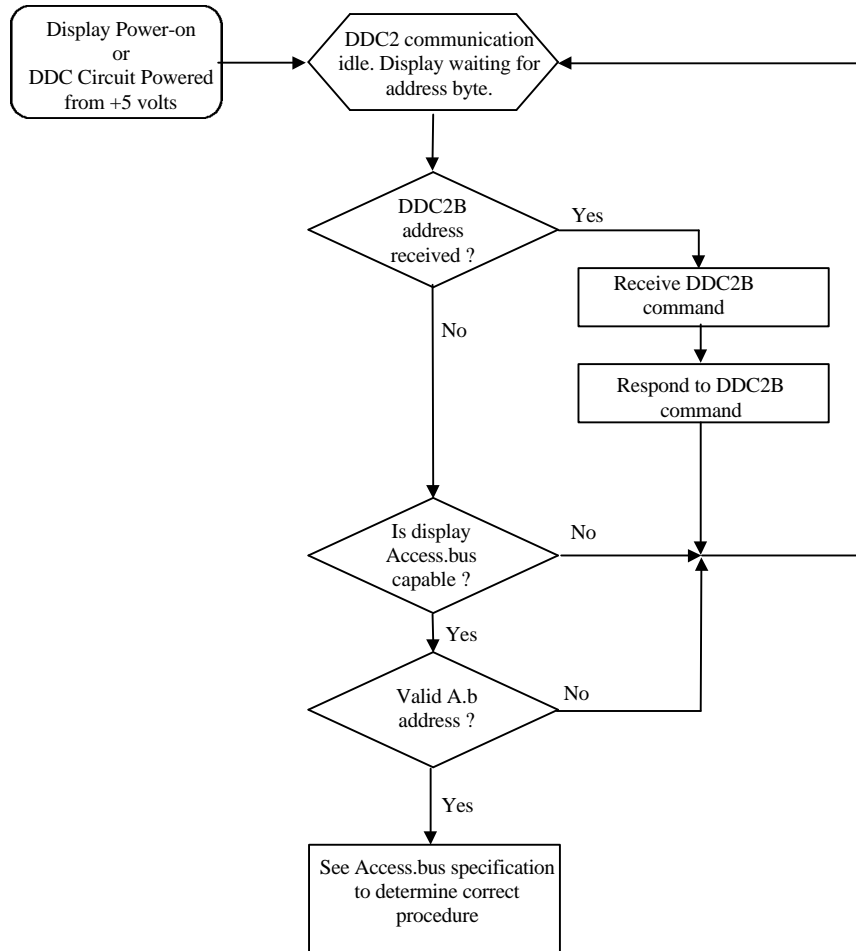
5.2.1 Display

A FPD-2 display shall be DDC2 capable. DDC2 mode.

5.2.1.1 DDC Operation Level Selection : Display View Flow Chart

The following flow chart is for guidance only, the text description of DDC operation takes precedence.

Note: For details of DDC2B to DDC2AB and DDC2B to DDC2B+ mode changes and ACCESS.bus operation, refer to Appendix E and the ACCESS.bus monitor device protocol specification.



5.2.2 Host System

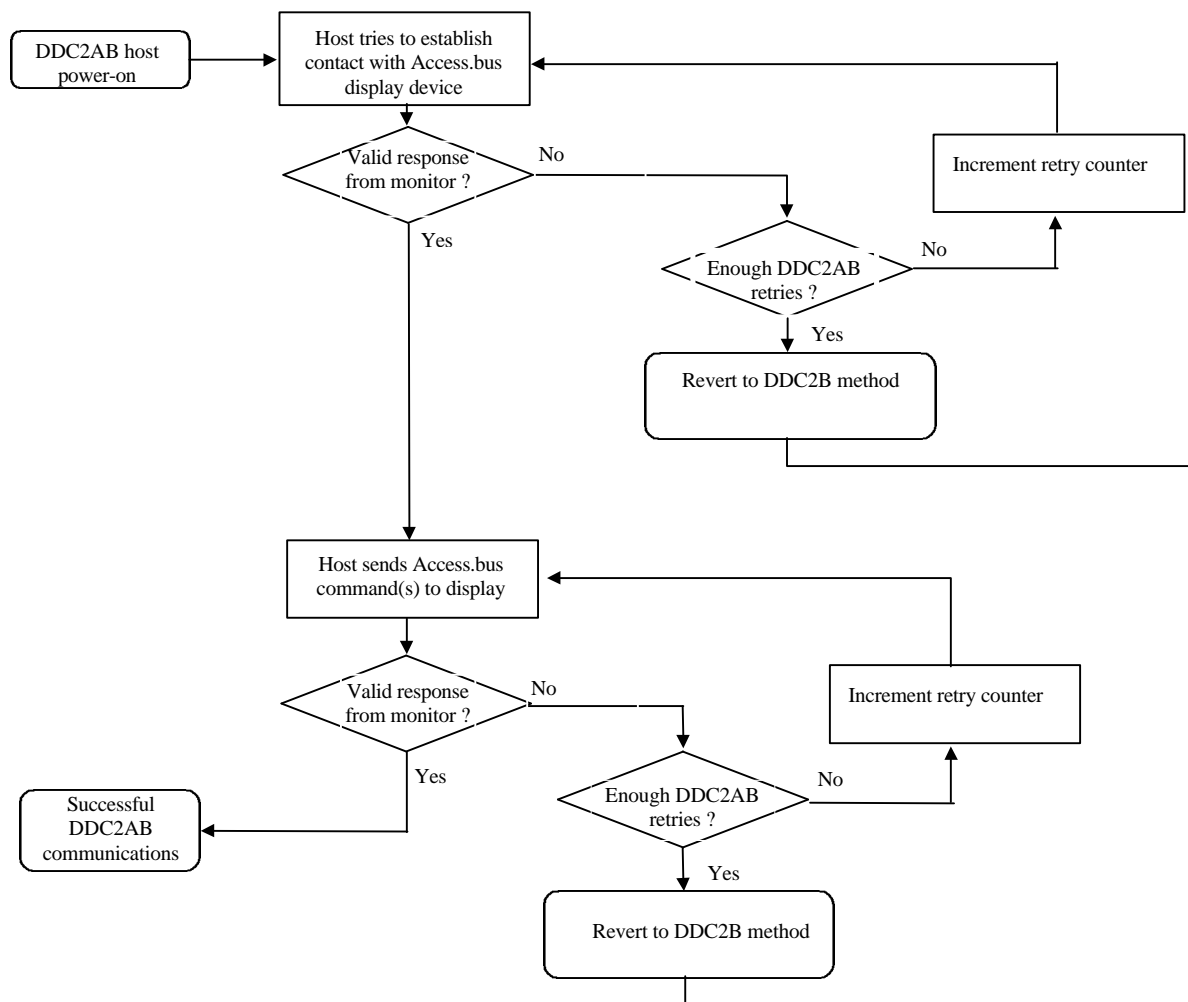
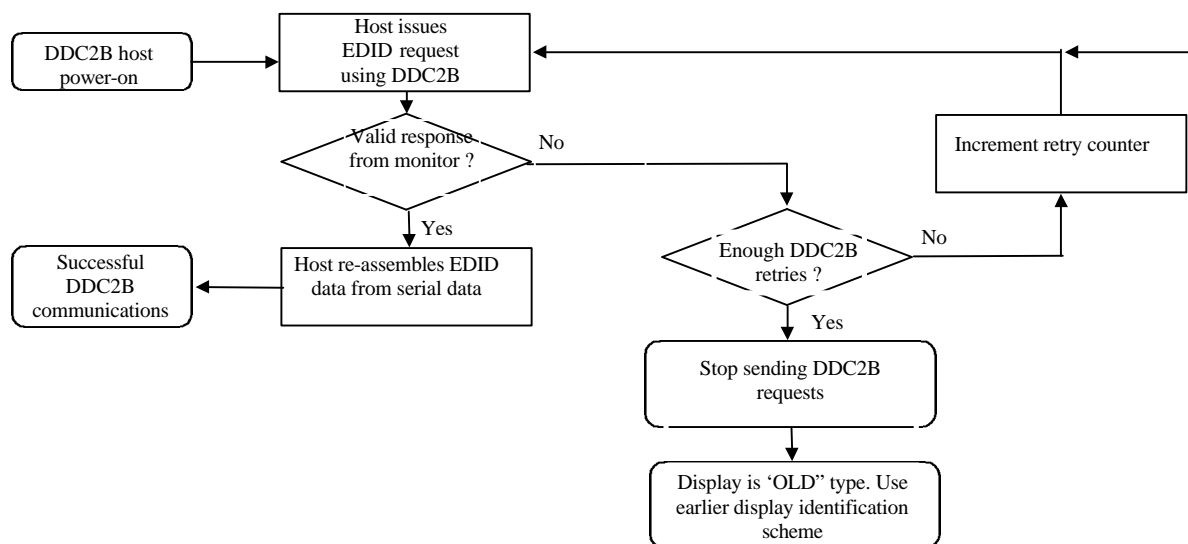
5.2.2.1 DDC2B Capable Host

The DDC2B system should issue a request for the EDID data using DDC2B protocol, to the FPDID defined I2C address location. If no valid response is received then the host shall stop sending DDC2B requests to the display and assume that the display is of type “Old”.

Note : At least one retry should be attempted before reaching a decision.

5.2.2.2 DDC Operation Level Selection : Host View Flow Charts

Note : In order to respond, the display DDC circuit must have power - supplied either from the display or by + 5 volts on signal # 3 of the FPDID-2 connector from the system. It is recommended that new monitor designs use the +5 volts supplied by the host.



6. Physical Connections

6.1 Display Host Graphics Controller

6.1.1 Purpose

To provide a standard mechanical and electrical interface between the display and host graphics controller through which DDC communications can pass. This document specifies the interface through the standard 15-pin VGA connector. The VESA EVC standard specifies the interface in the EVC connector. The VESA P&D standard specifies the interface in the P&D connector. The VESA FPD-2 standard (under development) specifies the interface in the FPD-2 connector. See appendix A for summaries. Other types of connector may be utilized, however, their definition is outside the scope of this standard.

6.1.2 Mechanical - VGA Connector

The mechanical specification for the DDC is backwards compatible with the standard 15-position VGA-type connector with the following exceptions.

- Socket # 9 shall be recessed by 0.050 inches for DDC compliance. Socket to retain contact capability.
- The host side connector color, plastic part, shall be “royal blue” to clearly indicate that socket is DDC compatible and provides a +5 volt supply.

Suitable connectors are available from a number of sources, the following are listed for reference. This does not imply that VESA recommends or approves these particular connectors :

• AMP	p/n	787066-1	787066-2	787506-1
• Molex	p/n	89263-7**	89141-70**	89046-70**

6.1.3 Mechanical - EVC Connector

See the VESA EVC standard for details and Appendix A of this standard for summary of DDC related pins.

6.1.4 Mechanical - P&D Connector

See the VESA P&D standard for details and Appendix A of this standard for summary of DDC related pins.

6.1.5 Mechanical - FPD-2 Connector

See the VESA FPD-2 standard for details and Appendix A of this standard for summary of DDC related pins.

6.1.6 Electrical

6.1.6.1 General

Display should provide a 47 K Ω pull up resistor to +5 volt dc on the clock (SCL) line.

Graphic controller boards should provide pull-up resistors of ≥ 1.5 K Ω and ≤ 2.2 K Ω to a +5 volt reference or a 3 mA current source for the SCL and SDA open drain signals.

All the SDA and SCL pull up resistors should be located within the host system except for the 47 K Ω pull up resistor on the SCL line specified above.

The system unit or graphic card shall supply +5 volts (+/- 5%) on socket # 9 (VGA connector) and pin #

28 (EVC connector). The required current capability is dependent on the specific level of DDC being implemented as defined in Appendix A.

Note 1 : In the case of a DDC1 only host system, the SCL line should be left open (no pull up resistor) in the host.

Note 2 : Appendix C is extracted from the Access.bus Specification, Version 3.0 for reference, all designers should consult the latest version of the Access.bus Specification for the full text and to ensure that DDC2 data (pin # 12 of the VGA connector and pin # 26 of the EVC connector) and clock (pin # 15) of the VGA connector and pin # 27 of the EVC connector) lines meet the electrical specifications defined in the latest version of the ACCESS.bus specification.

6.1.7 Timing

6.1.7.1 DDC1 Timing

Data is clocked on the rising edge of the VCLK and shall be valid 30 microseconds after the rising edge, it shall remain valid until the next rising edge. The minimum time between the falling edge of the clock and the next rising edge shall be 20 microseconds. The minimum clock pulse high time shall be 20 microseconds.

The DDC1 data shall be clocked with nine clocks per byte, the data bit generated on the ninth clock is an acknowledge bit that should be discarded by the host. The data for the ninth bit can be either high or low but shall be consistent for all bytes from a particular display.

It is recommended that the ninth bit be high to ensure a data line transition even if data bits are zero.

For DDC1 operation, the VCLK shall start at the normal frame frequency. Once data is sensed on the data line, the VCLK may be increased to a maximum of 25 KHz.

Warning

If no data is received at the normal video frame frequency then the display may be of type “Old”. Type “Old” monitors may be damaged if a higher than normal vertical frequency is applied.

6.1.7.2 DDC2 Timing

Data is synchronized with the clock signal and timing shall comply with the I²C and ACCESS.bus specifications.

Refer to I²C and ACCESS.bus specifications for details.

6.2 Host ACCESS.bus Û Graphic Controller Connection

6.2.1 Purpose

To provide a standard mechanical and electrical interface between the host ACCESS.bus signals located on the system board and the DDC signals on the graphics controller. In case the ACCESS.bus controller and display connector are located on different PCBs or otherwise, when applicable, the connector described below shall be provided on the graphics controller PCB.

6.2.2 Mechanical

The connectors on the graphic PCB and the host shall be 5 pin, 0.1 inch pitch, square post, straight, male connectors. On a graphics board it shall be located within 50 mm from the end of the board carrying the VGA connector and a maximum of 20 mm from the top edge of the board.

Cabling shall have mating 5 pin connectors.

Connectors are readily available from numerous sources.

Refer to Appendix B for pin allocation.

Note : The EVC standard uses a different connector to implement this function - refer to the EVC standard for details.

6.3 Display

6.3.1 DDC Line Termination

For a DDC1 only host, the SCL line shall not be connected at all within the host system. The SCL line will be kept high by the pull-up resistor in the display while the display is powered on.

7. Data Transfer Protocols

7.1 DDC1

A uni-directional channel from display to host. The 128-byte EDID is continuously transferred from the display to the host on the serial data line (SDA), clocked by Vsync.

7.2 DDC2B

A uni-directional channel from display to host. The host computer uses base level I²C commands to read information from a display with a slave address.

Specific types of displays contain EDID at specific I2C device addresses and word addresses within the device. These are defined in table 7.1 below.

Display type	EDID base address	Data size	EDID extension address	Data size
Monitor using a VGA or EVC connector	A0h Device 00h start address	128 bytes	A0h device 80h start address	128 bytes
P&D compatible display	A2h device 00 start address	256 bytes	A4 device 00h start address	256 bytes
FPGI-2 compatible display	A6h device 00 start address	256 bytes	A8h device 00 start address	256 bytes

Table 7.1 - DDC2B device addresses

Note: It is possible that a monitor using a VGA or EVC connector may provide a EDID version 2 data structure at the A2h base address in addition to the EDID version 1 structure at the A0h base address. This is permissible so the display can provide the enhanced information defined in the Version 2 data structure. Monitors using an EVC connector must do this in order to be considered a P&D compatible display. See the EVC standard Version 2 for details

Basic operations for DDC2B access are as follows :

For systems compatible with DDC ver 2.0

Read EDID

Device A0h, start address 00h, read 128 bytes

If no valid response then display is not DDC capable

Optional Extended EDID blocks of 128 bytes each can be read at subsequent start addresses

e.g. A single optional EDID block can be read with the command :

Device A0h, start address 80h, read 128 bytes

Read VDIF

If implemented the VDIF follows immediately after the last EDID block. In the case of a single EDID block, the VDIF may be read as follows :

Device A0h, start address 80h, read VDIF block 0 (64 bytes)

Device A0h, start address C0h, read VDIF block 1 (64 bytes)

All bytes are obtained by consecutively reading from device address A0h with the read-bit set (i.e. A1h). In case of an error resulting in the need to re-transmit, the transmission must be started again from start address A0h.

For P&D compatible systems

Read EDID

Device A2h, start address 00h, read 256 bytes

If no valid response then at device A0h, start address 00h, read 128 bytes

If no valid response then display is not DDC capable

Optional Extended EDID extension of 256 bytes can be read at device A4h start address 00

For FPD-2 compatible systems

Read EDID

Device A6h, start address 00h, read 256 bytes

If no valid response then display is not DDC capable

Optional Extended EDID extension of 256 bytes can be read at device A8h start address 00

7.3 Additional DDC Protocols

Additional DDC communications protocols for purposes other than reading configuration information may be defined by VESA. Definitions of these protocols may reside in separate VESA standards.

Information about the existence of such protocols and their definitions can be obtained from VESA.

8. Compliance with this Standard

Compliance with the VESA DDC Standard requires that all the requirements of Sections 1 to 6 inclusive for whichever level of the DDC Standard is being implemented are met.

8.1 Existing Designs

Existing DDC Monitor and Graphic Sub-system designs will generally comply with the DDC Standard Version 1 Revision 0 only and not support the new features added in later versions of the DDC Standard.

8.2 New Monitor Designs

New DDC Monitor designs are recommended to comply with DDC Standard Version 2 Revision 1 (or later) but some companies may choose to only implement the DDC Standard Version 1 Revision 0 features.

8.3 New Graphic Sub-system Designs

New DDC Graphic Sub-systems designs are recommended to comply with DDC Standard Version 2 Revision 1 (or later) but some companies may choose to only implement the DDC Standard Version 1 Revision 0 features.

Note : New DDC compliant Graphic Sub-system designs should check the EDID version and revision number fields to determine the appropriate way to decode the EDID.

9. Appendix A - Display / Host Graphic Controller Connection

9.1 15-pin D-type (VGA) Connector

The mechanical specification for the display to host graphic controller is backward compatible to the standard 15-pin, VGA-type connector. If the +5 volts is present (required for all host DDC implementations compliant with DDC Version 2 Revision 0 and later) then the connector shall meet the additional requirements specified in Section 5.1.2

Pin #	Standard VGA	DDC1 Host	DDC2B Host	DDC2B+ or DDC2AB Host	DDC1/2 Display
1	Red video	Red video	Red video	Red video	Red video
2	Green video	Green video	Green video	Green video	Green video
3	Blue video	Blue video	Blue video	Blue video	Blue video
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
5	Test (ground)	Return	Return	Return	Return
6	Red video return	Red video return	Red video return	Red video return	Red video return
7	Green video return	Green video return	Green video return	Green video return	Green video return
8	Blue video return	Blue video return	Blue video return	Blue video return	Blue video return
9	No connection (mechanical key)	+5 volt supply (mandatory supply)	+5 volt supply (mandatory supply)	+5 volt supply (mandatory supply)	+5 volt load (optional use)
10	Sync. return	Sync. return	Sync. return	Sync. return	Sync. return
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	Bi-directional data (SDA)	Bi-directional data (SDA)	Bi-directional data (SDA)
13	Horizontal sync.	Horizontal sync.	Horizontal sync.	Horizontal sync.	Horizontal sync.
14	Vertical sync.	Vertical sync.	Vertical sync.	Vertical sync.	Vertical sync.
15	Monitor ID bit 3	Open	Data clock (SCL)	Data clock (SCL)	Data clock (SCL)

Table 9.1 - 15-pin D-type Connector Pinouts

System units shall supply +5 volts $\pm 5\%$ on pin # 9, the required current capability is dependent on the specific level of DDC being implemented as follows :

DDC Level	Required Current Capability
DDC1	Minimum of 50 mA, maximum of 1 A
DDC2B	Minimum of 50 mA, maximum of 1 A
DDC2B+	Minimum of 50 mA, maximum of 1 A
DDC2AB	Minimum of 300 mA, maximum of 1 A

Table 9.2 - Pin 9 Current Capabilities

9.2 EVC Connector

DDC signals are carried on the following pins of the EVC connector. Full description of this connector specified in VESA EVC Standard.

Pin	Signal
25	DDC return
26	DDC data (SDL)
27	DDC clock (SCL)
28	+5 V dc

Table 9.3 - DDC Signals on EVC Connector

The +5 volt supply shall comply with the requirements specified in the EVC standard.

9.3 P&D Connector

DDC signals are carried on the following pins of the P&D connector. Full description of this connector specified in VESA Plug and Display Standard

Pin	Signal
25	DDC return
26	DDC data (SDL)
27	DDC clock (SCL)
28	+5 V dc

Table 9.4 - DDC Signals On P&D Connector

The +5 volt supply shall comply with the requirements specified in the P&D standard.

9.4 FPDI-2 Connector

DDC signals are carried as optional signals on the following pins of the FPDI-2 connector. Full description of this connector specified in VESA Flat Panel Display Interface-2 Standard

Pin	Signal
1	DDC data (SDL)
2	DDC clock (SCL)
3	+5 V dc
6	DDC return

Table 9.5 - DDC Signals On FPDI-2 Connector

The +5 volt supply shall comply with the requirements specified in the EVC standard.

9.5 Host ACCESS.bus / Graphic Controller Connection

The connectors on the graphics card and host for ACCESS.bus connection shall be single in-line, 0.1 inch center-center connectors with pin assignment as follows :

Pin #	Assignment
1	Ground
2	Mechanical key
3	SDA
4	+5 volt ACCESS.bus supply
5	SCL

Table 9.6 - ACCESS.bus Header Connector

10. Appendix B

10.1 Access.bus Implementation Notes

Note: The following is copied from the Access Bus Specification V3.0 for guidance but a complete review of the current Access Bus specification is recommended to all developers. This section is not considered part of the VESA DDC standard.

From Access Bus Spec., 1.2 General Characteristics

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a current source or pull up resistor. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open collector in order to perform the wired-AND function. Data on the ACCESS.bus can be transferred at rates up to 100 Kbits/s in the standard mode. The number of OFF-board interfaces connected to the bus is dependent on the bus capacitance limit of 1000 pF, the overall bus length of 10 meters, and the current available to power the devices.

From Access Bus Spec., 1.7 Cabling and Connectors

The OFF-board ACCESS bus cable has the following wire sizes:

SDA and SCL wire size AWG # 28

Gnd and +5V wire size AWG # 26

The capacitance of the SCL and SDA conductors shall be less than 70 pF per meter between one conductor and other conductors connected to a shield.

From Access Bus Spec., 1.7.5 Pull-ups and Series Resistors

The host provides a pull-up resistor or a 6mA current source for the SCL and SDA open drain signals. The pull-up resistors or the current sources provide 6mA per line to pull the line to HIGH logic level. The minimum pull-up resistor is 820 Ohms.

A 51 Ohm maximum series resistor is connected between the SDA and SCL pins on each device and the corresponding signals on the OFF-board ACCESS bus. This resistor smoothes the bus signals and offers additional ESD (electrostatic discharge) protection to the device. Two clamping diodes to GND and +5V offer additional ESD protection. The diodes are needed only if they do not exist in the devices controller.

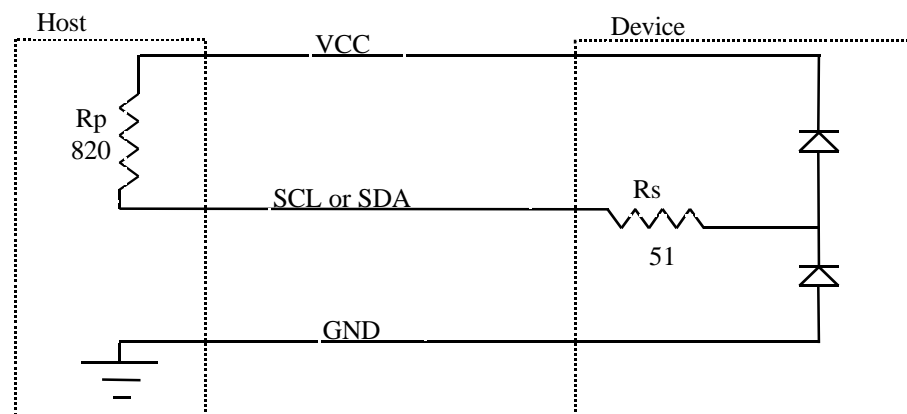


Figure 1.14: Pull-up and serial resistors for the SDA and SCL lines

10.2 Design Considerations

This section is not a formal part of the Monitor Device Protocol specification. It is meant as an aid for monitor and computer system designers implementing ACCESS.bus.

10.2.1 Monitor Host Detection

The VESA Display Data Channel (DDC) specification defines a multitiered protocol, allowing system and monitor designers to select the most appropriate feature set. DDC provides four levels of host implementation, monitor data stream clocked by Vsync (DDC1), I²C master (DDC2B), ACCESS.bus (DDC2AB) and point to point ACCESS.bus (DDC2B+).

The monitor must automatically determine the host system implementation. If the monitor is attached to a system that is not DDC compliant, it should continue to support existing industry standards for monitor identification using the two identification pins not utilized by DDC. This section discusses compliance with the VESA DDC specification only, OLD type systems are not discussed.

The monitor needs to determine the type of host system:

DDC1 or OLD type host
DDC2B host (Host is master, monitor is always slave)
DDC2AB (or DDC2B+) host ACCESS.bus

The sequences of events are as follows:

Step 1: - DDC1/2B detection

Assume monitor is connected to a DDC1 or OLD type host. Output EDID information clocked by Vertical Sync.

If SCL activity detected switch to DDC2B mode. Emulate EDID memory device. Set monitor to I²C slave address A0 / A1h. Go to step 2

Step 2: - DDC2AB detection

The monitor determines if an ACCESS.bus Host is present by detecting valid ACCESS.bus Reset command (op-code F0h) directed to address 6Eh. If the monitor determines that ACCESS.bus Host is present it will, reset device address to 6Eh, disable DDC1/2B mode and enable ACCESS.bus mode.

Monitors check for Host presence by checking activity at address 6Eh. If the monitor cannot detect both address A0h and 6Eh at the same time, the monitor should periodically switch from address A0h to 6Eh to test if the ACCESS.bus Host is present and switch back to A0h if the host is not detected. The monitor should switch from A0h to 6Eh approximately every 500 mS and stay at address 6Eh for a minimum period of 200 mS or until it detects an ACCESS.bus reset command.

While temporarily at address 6E, the monitor should watch for a Reset message to address 6Eh from the host address, 50h. The monitor should also try sending an Attention message to address 50h. If this message is not acknowledged, the monitor should switch back to address A0h and recheck at next period.

Note : Whenever an ACCESS.bus host attempts to control a DDC2AB monitor, it should start by continuously sending Reset commands to the monitor for a period of 1 second or until the Reset command is acknowledged by the monitor.

10.2.2 ACCESS.bus Host Monitor Detection - Host Boot Time

The VESA DDC specification defines two classes of monitors, DDC1/2B and DDC1/2AB. DDC1/2B monitors store monitor capability information in an I²C device. Host systems obtain the monitor's EDID information by performing a master memory read of the 128-byte EDID structure. DDC1 is read back only, this type of monitor does not support remote control. DDC1/2AB monitors are ACCESS.bus devices. They can provide greater capability information and allow the host to control monitor features remotely. All DDC compliant monitors support DDC1/2B, support for DDC1/2AB is optional.

ACCESS.bus Plug and Play host systems should support the attachment of three different types of monitor.

Non Plug and Play monitor
DDC1/2B - Slave I²C
DDC1/2AB - ACCESS.bus

The sequence of events is as follows:

Step 1: - Stuck bit detection

IF the ACCESS.bus micro controller allows I/O stuck-at testing, test both clock and data lines for stuck high or stuck low problems.

IF a failure occurs disconnect the clock and data lines from the monitor. Abort attempt to communicate with monitor.

DDC monitors power up in a data streaming mode, clocked by vertical sync. The monitor automatically terminates this mode when it detects I²C clock transitions. It is good design practice to toggle the clock line before ACCESS.bus initialization.

OLD type of monitors may interfere with the ACCESS.bus clock and data lines. The DDC specification reassigns two VGA ID lines as the I²C clock and data signals. OLD type of monitors selectively ground the ID lines to encode monitor type.

Step 2: - DDC2AB detection

For a period of 1 second or until the message is acknowledged by the monitor the host sends continuous Reset commands to address 6Eh.

IF the last Reset message is acknowledged by the monitor, a DDC1/2AB monitor is detected. The Monitor has full ACCESS.bus capability.

ELSE Go to step 3.

Step 3: - DDC2B detection

Attempt to read the VESA EDID information from the monitor. Select slave address A0h. Attempt to read the VESA EDID structure starting at memory address 0h. EDID data is 128 bytes long beginning at memory address 00h. Use the auto increment feature to read back EDID. The EDID header is 00 FF FF FF FF FF FF 00 (in hex).

IF EDID data is returned, a VESA DDC1/2B type monitor is attached.

ELSE monitor does not support VESA DDC Go to step 4.

DDC1/2B class monitors store EDID data in an I²C device. Host support for DDC1/2B requires I²C master transmitter and master receiver functions.

Step 4: OLD type of monitors

Use industry standard methods to determine monitor type.

10.2.3 ACCESS.bus Host Monitor Detection - Hot Monitor Attach

DDC2AB monitors may be connected to ACCESS.bus host after the system is powered up. When the monitor is first powered-on, it will be in DDC1 communication mode., outputting information as clocked by VSYNC. When it detects the presence of SCL it switches to DDC2B mode. In this mode it responds as a slave device to memory reads at A0/A1h. When the monitor detects that it is connected to an ACCESS.bus host, it sets its base address to the ACCESS.bus power up default address 6Eh. Then the monitor sends the standard ACCESS.bus Attention message. When the host recognizes this message it sets the monitor to an unused address and performs normal ACCESS.bus messaging.

10.2.4 Monitor Isolation

The VESA DDC communication interface redefines two of the existing VGA ID pins as I²C clock and data signals. These signals were chosen to minimize compatibility problems with existing monitors. However, if a monitor grounds any of the ID lines used for DDC communication, the ACCESS.bus interface is rendered inoperable. The VGA specification indicates monitor type by grounding different combinations of ID pins. If the system designer needs to support OLD type of monitors, some form of monitor disconnect is necessary.

The VESA DDC specification defines a 5 pin connector between the host motherboard and video controller card. The main purpose of this connector is to connect an ACCESS.bus host system to a DDC compliant add in Video display adapter. If manual disconnect is acceptable, this connector may be used to isolate interfering monitors. Another possibility is to use a bi-directional hardware switch. This allows hardware isolation under software control, and may be a better strategy for Plug and Play systems.

10.2.5 DC Loading

ACCESS.bus devices are specified to sink 6mA. To maximize transfer speed, the host uses low value pull-up resistors to source approximately 6mA. The DC loads of add-on video cards and monitors must be taken into account by the system designer.

VESA specifies a 47k pull-up on the monitor clock line. This increases the ACCESS.bus clock sink requirements by approximately 100µA. This is equivalent to 10 standard ACCESS.bus devices, this small value may generally be ignored. However, if more than one monitor is likely to be connected, the motherboard pull-up resistors should be increased to keep clock line sink current from exceeding 6mA.

Add on video adapter cards, that support DDC, are designed to work as stand alone DDC1/2B interfaces or with ACCESS.bus hosts. This means the adapter card must provide pull-up resistors on the clock and data lines. The VESA specification requires adapter cards to use 1.5KΩ → 2.2KΩ pull-ups when not connected to an ACCESS.bus controller.

10.2.6 Multiple Monitor Support

In multiple display systems the displays may be attached to more than one video controller. The video driver needs to determine how the displays are connected. The ACCESS.bus allows individual displays to be identified, however, it does not provide a means to associate a display with a particular video controller.

The Monitor Timing Message provides a convenient method to do this. The Video driver changes the timing mode of one of the video controllers. The driver can then send a Get Timing Report command to all monitors. The monitor attached to that controller will send a Monitor Timing Message corresponding to the correct mode. The video device driver can use this information to determine which monitors are attached to which controllers.

10.2.7 Monitor Change Notification

One of the advantages of the ACCESS.bus, is automatic host notification when devices are plugged in. This is an important feature in Plug and Play systems.

Monitors that are only DDC1/2B compliant do not have this capability. ACCESS.bus host systems should periodically test for the presence of DDC1/2B monitors. This requires testing for the presence of a slave memory device at address A0h. This should be done as part of the other ACCESS.bus housekeeping tasks. This makes it easy to detect monitor attachment or removal.

10.2.8 Video Switch Boxes

Video switch boxes allow a single display to be attached to more than one computer system. Switch boxes vary in sophistication. System designers should assume switching a monitor to a different host completely disconnects it from other hosts.

The previous Design Considerations recommend ACCESS.bus hosts detect disconnect and attachment of both DDC1/2B and DDC1/2AB type monitors. Video device drivers should be designed to assume the video display may be connected and disconnected at any time. The device driver should ignore monitor disconnect. It should not change video capabilities until it receives a monitor connect message. This minimizes the time it takes to recognize and resynchronize when the monitor is reconnected.

11. Appendix C - DDC2B Host Implementation Application Note:

This appendix is offered for information only and does not form part of the DDC standard. The techniques specified here are not the only nor, necessarily, the best implementations.

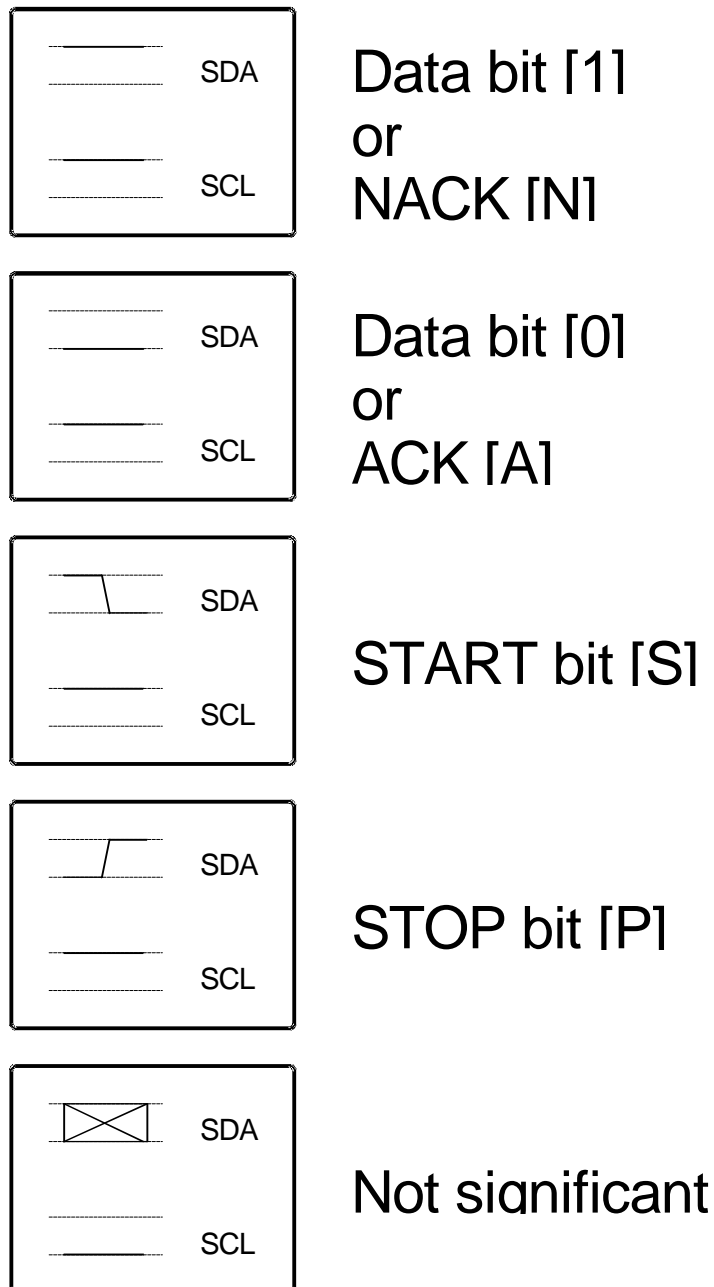
11.1 Purpose

The application note is intended to aid graphic sub-system designers wishing to implement DDC2B compliant Hosts that achieve a high level of compatibility with displays from different manufacturers.

If the host cannot achieve full compliance with the I²C Bus spec., some suggestions are given to minimize this limitation.

11.2 Notation

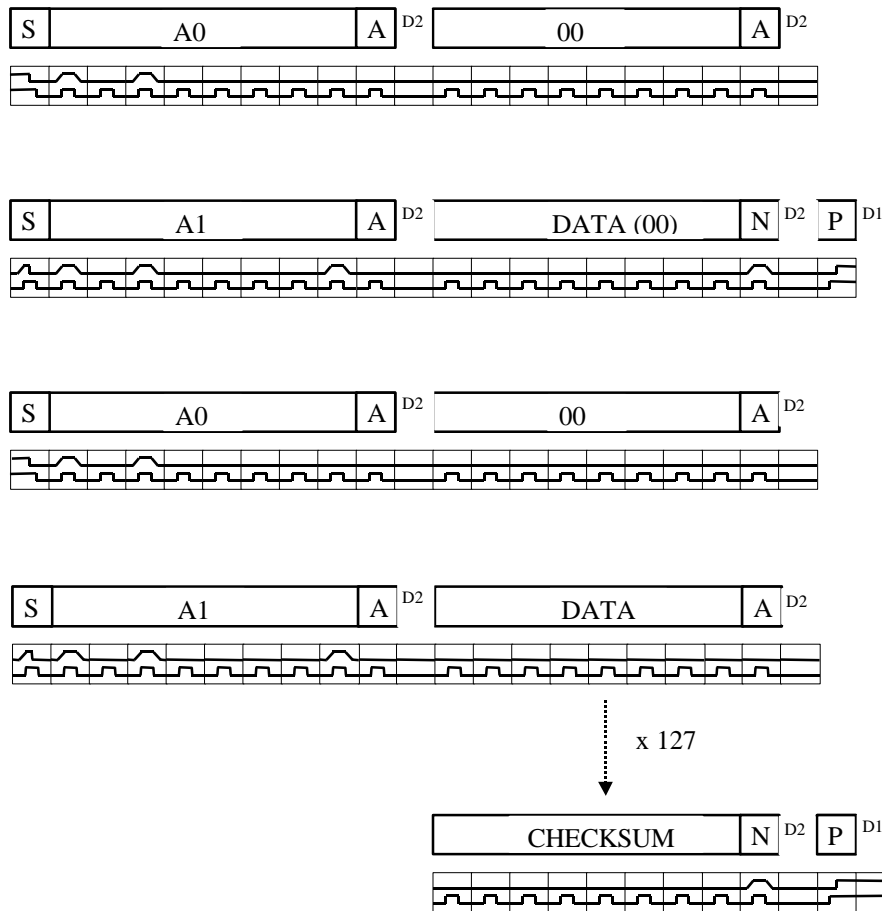
The I²C Bus Specification has a standard notation as shown below:



Note : The I²C Bus specifies that the SCL Line can be stretched low by the slave in order to slow down the communication.

11.3 Typical Command Sequence

Here is shown a typical I²C sequence from the DDC2B host to the display to get the EDID data:



Note : D1 and D2 are delays defined later in this appendix.

11.3.1 Comments on the sequence, line by line

11.3.1.1 First and Second Lines

The host reads the first byte of the EDID to cause the monitor to switch from DDC1 to DDC2B mode.

11.3.1.2 Third, Fourth and Fifth Lines

- The Host reads the 127 data bytes plus the checksum byte of the EDID.

Note: To minimize glitches on I²C Bus lines, one way is to add a 100 Ohm serial resistor (refer to I²C specification) as close as possible to the SDA & SCL pins of the graphic controller (note that it may be preferred to implement this in monitor). This will create an RC filter

11.3.2 Suggestions about Error Recovery

The Host should check if the display acknowledges its own slave address and any received data byte.

If the display fails, the host should initially terminate the current line-sequence and then should try, at least once again, the full sequence. Communications with the display should only be considered to have failed if the retry(s) failed.

11.4 Timing

D1 is the typical delay the host should implement between a STOP and a START bit.

D2 is not useful for I²C Bus compliant Hosts which check if the display stretched the SCL line low.

11.4.1 I²C BUS Compliant Host

Note : An I²C bus compliant host has the capability to check for clock stretching:

Delay D1 should be 500 uS

Delay D2 is used as a time-out of 2 mS

Note : In the I²C Bus specification the maximum delay a slave can stretch a clock low is not defined but we recommend a time-out giving a maximum clock stretching delay of 2 mS, as defined in the Access Bus specification.

Since the standard I²C maximum communication speed is 100 KHz, it is good design practice to have BIOS code which is independent of the CPU speed.

12. Appendix D

This appendix is offered for information only and does not form part of the DDC standard.

12.1 Partial Protection against Hot-plugging of Monitor

The technique specified is recommended for new monitor designs where ‘hot-plugging’ of the monitor between different system units may be an issue.

Pin # 5 of the monitor VGA interface is defined as a ‘test line’. This is grounded in the host system to indicate to the monitor that it is connected. The monitor will detect if the VGA connector is unplugged since the ‘test line’ will either float high or be pulled high (dependent on particular monitor design). A ‘high’ condition on the test line will cause the monitor to take action(s) such as blanking video, entering test mode, displaying a “not connected” message, etc.

If a DDC capable monitor is ‘hot-plugged’ between host systems, then it is possible that no DDC communications will be possible without power cycling the monitor.

e.g. If a monitor has established DDC2 communications with a host system but is then plugged to a host system only capable of DDC1 communications.

An additional use of the ‘test pin’ is recommended - when a monitor is in DDC2 communications mode and detects a low → high transition on the test line, it should revert to DDC1 communications.

Note: A similar function may be accomplished when using EVC by, for example, connecting the test line from the monitor to the synchronization signal return.

12.2 Hot-plugging a Plug & Display Monitor

Hot plugging considerations for this type of display are referenced in the VESA Plug & Display Standard and the VESA EVC Standard Version 2.

13. Appendix E - DDC Monitor Control

13.1 Display/Host Communication Channels

13.1.1 DDC2B+ Communications

A point to point, bi-directional, channel between the display and the host system. The same set of commands used in DDC2AB allows the host to read the EDID and / or VDIF information and to control display parameters. However, the host interface is simpler than DDC2AB, and may be implemented only by software (bit-banging). DDC2B+ does not support the connection of additional ACCESS.bus devices to the system, but could support the connection of additional I²C devices.

13.1.2 DDC2AB Communications

A multi-master, bi-directional, channel between the display, the host system and other ACCESS.bus devices. A set of commands based on the ACCESS.bus command structure allows the host to read the EDID and/or VDIF information, control display parameters, and communicate with other devices plugged to the ACCESS.bus.

13.2 Monitor Control Host Types

13.2.1 DDC2B+ Host

Systems capable of communicating with the display using DDC2B or ACCESS.bus commands. The DDC2B+ system uses a point to point, bi-directional, channel between the display and the host system. The host interface is simpler than that required for DDC2AB and may be implemented by software 'bit-banging' on two bi-directional pins. DDC2B+ does not support the connection of additional ACCESS.bus devices to the system, but may support the connection of additional I²C devices.

13.2.2 DDC2AB Host

Systems capable of communicating with the display using DDC2B or ACCESS.bus commands and capable of communicating with other devices plugged to the ACCESS.bus.

13.3 Normal Operation

In a DDC2B+ (emulated ACCESS.bus) or DDC2AB (ACCESS.bus) capable system the host determines if the display is also DDC2AB capable by trying to establish contact. If contact is not established, then the host should revert to the simpler protocol and read the I²C memory location to retrieve EDID or VDIF data.

13.3.1 DDC2B+ Capable Host

First, the DDC2B+ capable host shall try to establish contact with an ACCESS.bus display device. If no valid response is received then the host shall issue a request for the EDID data using DDC2B protocol. If the host is P&D or FPD-2 capable, the request should be made to the P&D or FPD-2 defined I²C address location. If no valid response is received or the host is not P&D or FPD-2 capable, the host shall issue a request for EDID data using DDC2B protocol at the default DDC I²C location of A0h. If no valid response is received then the host shall stop sending DDC2 requests to the display and assume that the display is of type "Old".

Note : At least one retry should be attempted before reaching a decision.

13.3.2 DDC2AB Capable Host

First, the DDC2AB capable host shall try to establish contact with an ACCESS.bus display device. If no valid response is received then the host shall issue a request for the EDID data using DDC2B protocol. If the host is P&D or FPD-2 capable, the request should be made to the P&D or FPD-2 defined I²C address

location. If no valid response is received or the host is not P&D or FPD1-2 capable, the host shall issue a request for EDID data using DDC2B protocol at the default DDC I2C location of A0h. If no valid response is received then the host shall stop sending DDC2 requests to the display and assume that the display is of type “Old”.

Note : At least one retry should be attempted before reaching a decision.

13.4 DDC2B+ and DDC2AB Data Transfer Protocol

A bi-directional communications channel. Uses the ACCESS.bus base protocol and the specific command set for display devices.

DDC2AB compliant displays shall transfer the EDID via the EDID Capability String as defined in Section 7 (paragraph 7.3.5.1) of the ACCESS.bus specification.

DDC2AB compliant displays shall transfer the VDIF via the VDIF Capability String as defined in Section 7 (paragraph 7.3.5.2) of the ACCESS.bus specification

These commands are part of the ACCESS.bus specification Version 3.0. In addition to the standard ACCESS.bus protocol messages, specific commands and data structures are defined to support the control of a generic display device.

14. Appendix F - Answers to Commonly Asked Questions

Ref #	Question	Answer
F1	Why is +5 volts on pin 9 mandatory for system units and/or graphic cards ?	Ref.: Section 5.1.4.1 It is becoming common for system management s/w to interrogate peripheral devices for product type and serial number as a form of asset management. This is usually scheduled for nighttime but if the monitor is powered off then no data can be collected. Providing +5 volts allows the DDC circuit in the monitor to remain active even when the monitor itself is powered off.
F2	Is +5 volts mandatory for portable computers ?	Ref.: Section 5.1.4.1 Portable computers which want to be able to claim compliance with VESA DDC standard version 2 must provide the +5 volt output.
F3	Is clock-stretching required ?	Ref. Section 2.2 Yes, compliance with VESA DDC standard requires that the requirements of the I ² C or ACCESS.bus specifications are met.